- **12-Bit-Resolution A/D Converter**
- **10-μs Conversion Time Over Operating Temperature**
- **11 Analog Input Channels**
- **3 Built-In Self-Test Modes**
- **Inherent Sample-and-Hold Function**
- **Linearity Error . . . $\pm$1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion Output**
- **Unipolar or Bipolar Output Operation (Signed Binary With Respect to 1/2 the Applied Voltage Reference)**
- **Programmable MSB or LSB First**
- **Programmable Power Down**
- **Programmable Output Data Length**
- **CMOS Technology**

DIP/SOP/SSOP
(TOP VIEW)

AIN0	1	20	V_{CC}
AIN1	2	19	EOC
AIN2	3	18	I/O CLOCK
AIN3	4	17	DATA INPUT
AIN4	5	16	DATA OUT
AIN5	6	15	$\overline{CS}$
AIN6	7	14	REF+
AIN7	8	13	REF−
AIN8	9	12	AIN10
GND	10	11	AIN9

description

The 2543 are 12-bit, switched- capacitor, successive-approximation, analog-to-digital converters. Each device, with three control inputs [chip select ($\overline{CS}$), the input-output clock, and the address input (DATA INPUT)], is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.
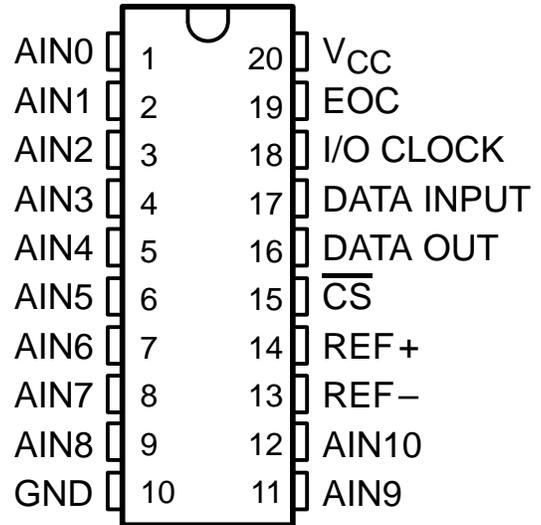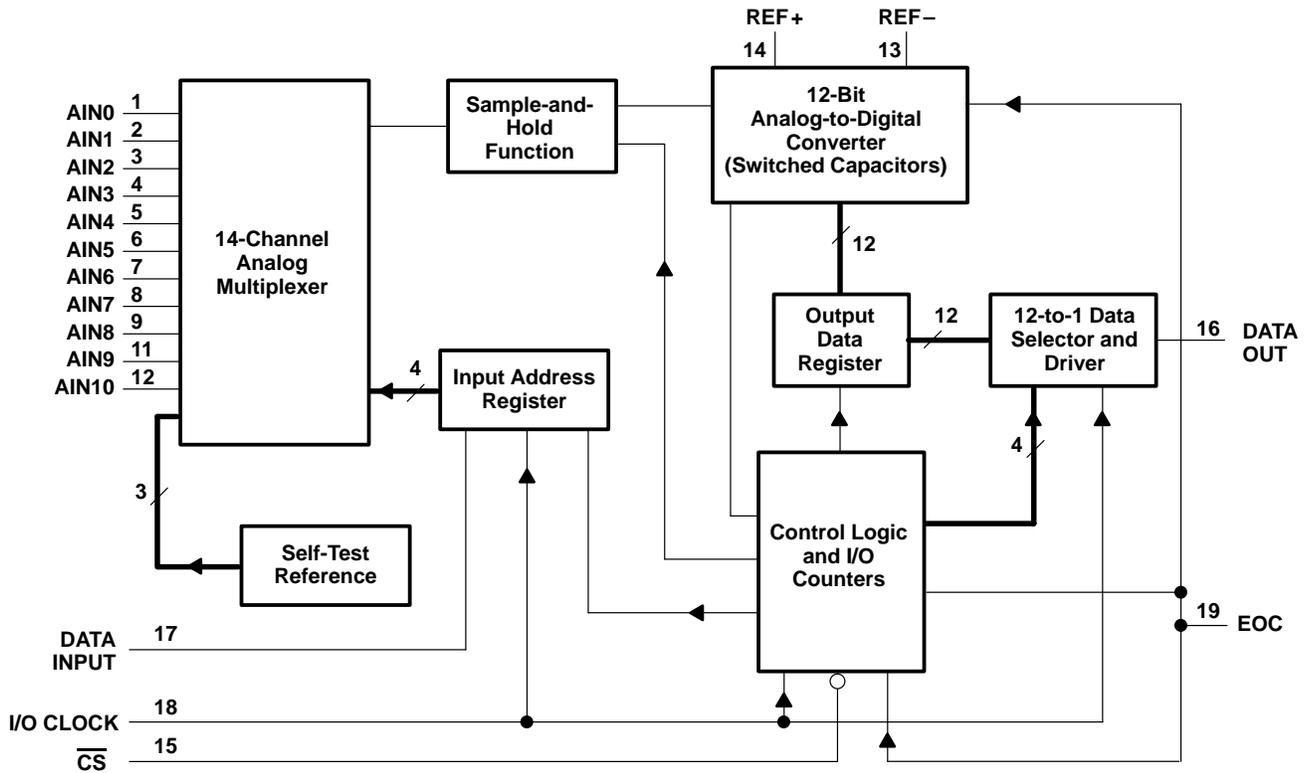
AVAILABLE OPTIONS

T_A	PACKAGE		
	DIP	SOP	SSOP
−40°C to 85°C	XD2543N	XL2543	XL2543-SS

functional block diagram

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AIN0 – AIN10	1 – 9, 11, 12	I	Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and be capable of slewing the analog input voltage into a capacitance of 60 pF.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB† value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and the data is ready for transfer.
GND	10		Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of the I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF+	14	I	Positive reference voltage The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal.
REF–	13	I	Negative reference voltage. The lower reference voltage value (nominally ground) is applied to REF–.
V_{CC}	20		Positive supply voltage

† MSB/LSB = Most significant bit / least significant bit

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −0.5 V to 6.5 V
Input voltage range, V_I (any input) .... −0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O .... −0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} .... V_{CC} + 0.1 V
Negative reference voltage, $V_{ref−}$ .... −0.1 V
Peak input current, I_I (any input) .... ±20 mA
Peak total input current, I_I (all inputs) .... ±30 mA
Operating free-air temperature range, TA: X*2543 .... −40°C to 85°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:   All voltage values are with respect to the GND terminal with REF− and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, $V_{ref−}$ (see Note 2)			0		V
Differential reference voltage, $V_{ref+} − V_{ref−}$ (see Note 2)		2.5	V_{CC}	V_{CC}+0.1	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Clock frequency at I/O CLOCK		0		4.1	MHz
Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 4)		100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 4)		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$ (see Figure 5)		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 5)		1.425			µs
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		120			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		120			ns
Transition time, I/O CLOCK high to low, $t_{t(I/O)}$ (see Note 4 and Figure 6)				1	µs
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	2543	0		70	
	2543	−40		85	°C

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF− convert as all zeros (000000000000).
3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
4. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.5 V to 5.5 V, $f_{(I/O\ CLOCK)}$ = 4.1 MHz (unless otherwise noted)

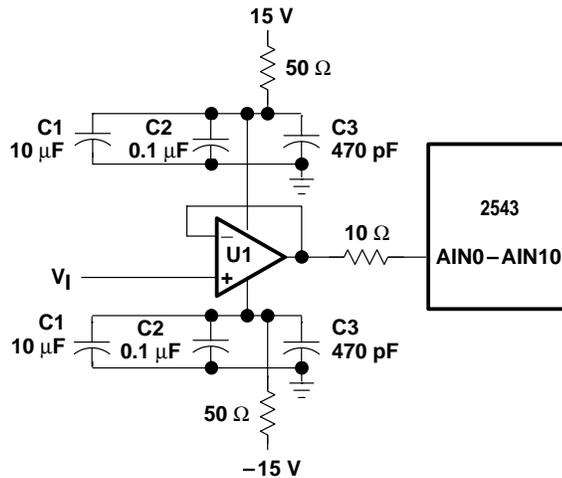| PARAMETER			TEST CONDITIONS		X*2543			UNIT
					MIN	TYP†	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = −1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −20 μA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 μA			0.1	
I_{OZ}	High-impedance off-state output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}		1	2.5	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}		1	−2.5	
I_{IH}	High-level input current		$V_I = V_{CC}$			1	2.5	μA
I_{IL}	Low-level input current		V_I = 0			1	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1	2.5	mA
$I_{CC(PD)}$	Power-down current		For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC} - 0.5$ V			4	25	μA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}				−1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND		1	2.5	μA
C_i	Input capacitance	Analog inputs				30	60	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

operating characteristics over recommended operating free-air temperature range,
$V_{CC} = V_{ref+}$ **= 4.5 V to 5.5 V,** $f_{(I/O\ CLOCK)}$ **= 4.1 MHz**

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)	See Figure 2			±1	LSB
E_D	Differential linearity error	See Figure 2			±1	LSB
E_O	Offset error (see Note 6)	See Note 2 and Figure 2			±1.5	LSB
E_G	Gain error (see Note 6)	See Note 2 and Figure 2			±1	LSB
E_T	Total unadjusted error (see Note 7)				±1.75	LSB
		DATA INPUT = 1011		2048		
	Self-test output code (see Table 3 and Note 8)	DATA INPUT = 1100		0		
		DATA INPUT = 1101		4095		
$t_{(conv)}$	Conversion time	See Figures 9 – 14		8	10	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 9 – 14 and Note 9			10 + total I/O CLOCK periods + $t_{d(I/O\text{-}EOC)}$	µs
t_{acq}	Channel acquisition time (sample)	See Figures 9 – 14 and Note 9	4		12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 6	10			ns
$t_{d(I/O\text{-}DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 6			150	ns
$t_{d(I/O\text{-}EOC)}$	Delay time, last I/O CLOCK↓ to EOC↓	See Figure 7		1.5	2.2	µs
$t_{d(EOC\text{-}DATA)}$	Delay time, EOC↑ to DATA OUT (MSB/LSB)	See Figure 8			100	ns
t_{PZH}, t_{PZL}	Enable time, CS↓ to DATA OUT (MSB/LSB driven)	See Figure 3		0.7	1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, CS↑ to DATA OUT (high impedance)	See Figure 3		70	150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 8		15	50	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 7		15	50	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 6		15	50	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 6		15	50	ns
$t_{d(I/O\text{-}CS)}$	Delay time, last I/O CLOCK↓ to CS↓ to abort conversion (see Note 10)				5	µs

† All typical values are at T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).

5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

6. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.

7. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.

8. Both the input address and the output codes are expressed in positive logic.

9. I/O CLOCK period = 1 /(I/O CLOCK frequency) (see Figure 7).

10. Any transitions of CS are recognized as valid only when the level is maintained for a setup time. CS must be taken low at ≤ 5 µs of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

6

PARAMETER MEASUREMENT INFORMATION

15 V

50 Ω

C1
10 μF

C2
0.1 μF

C3
470 pF

2543

AIN0−AIN10

U1

−

+

V$_I$

10 Ω

C1
10 μF

C2
0.1 μF

C3
470 pF

50 Ω

−15 V

LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10-μF 35-V tantalum capacitor	—
C2	0.1-μF ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain Hi-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

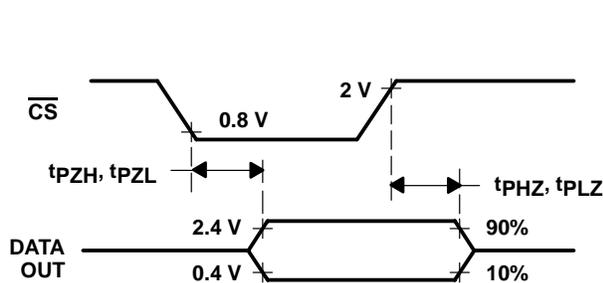**Figure 1. Analog Input Buffer to Analog Inputs AIN0−AIN10**

Test Point

V$_{CC}$

R$_L$ = 2.18 kΩ

EOC

C$_L$ = 50 pF

12 kΩ

Test Point

V$_{CC}$

R$_L$ = 2.18 kΩ

DATA OUT

C$_L$ = 100 pF

12 kΩ

Figure 2. Load Circuits

$\overline{CS}$

2 V

0.8 V

t$_{PZH}$, t$_{PZL}$

t$_{PHZ}$, t$_{PLZ}$

2.4 V

90%

**DATA
OUT**

0.4 V

10%
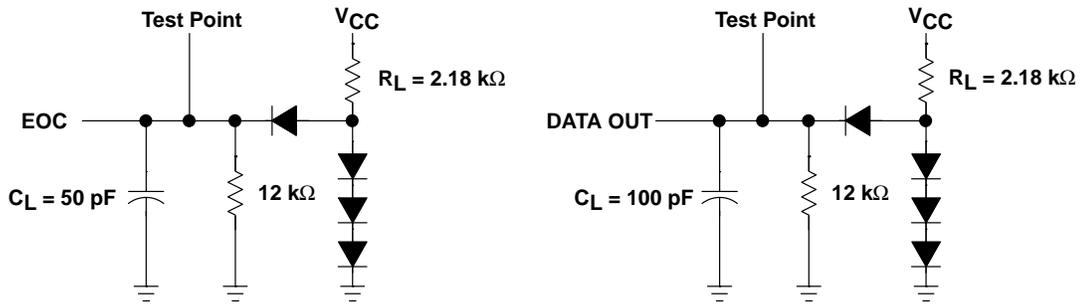
Figure 3. DATA OUT to Hi-Z Voltage Waveforms

**Data
Valid**

DATA INPUT

2 V

0.8 V
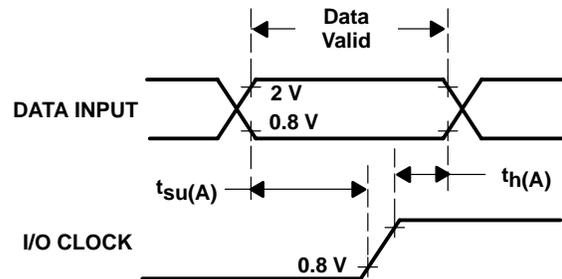
t$_{su(A)}$
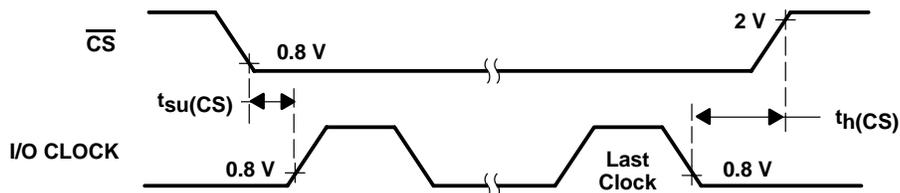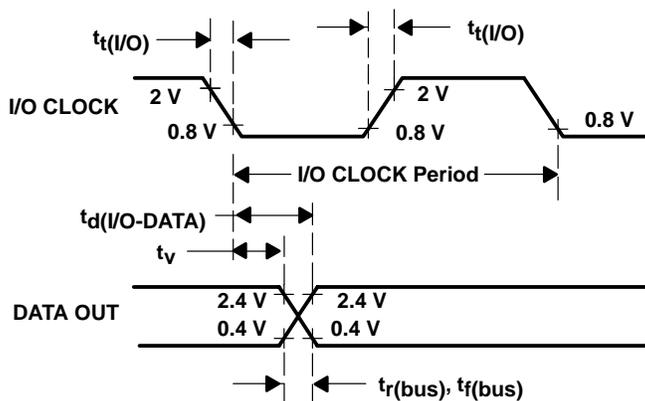
t$_{h(A)}$

I/O CLOCK

0.8 V

**Figure 4. DATA INPUT and I/O CLOCK
Voltage Waveforms**

7

PARAMETER MEASUREMENT INFORMATION

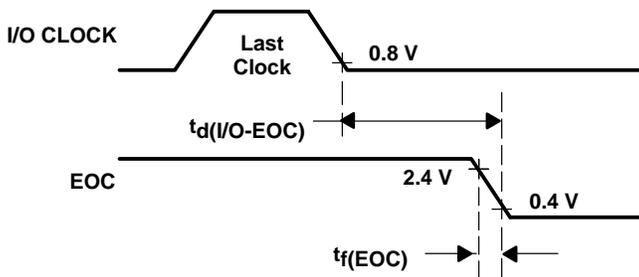NOTE A: To ensure full conversion accuracy, it is recommended that no input signal change
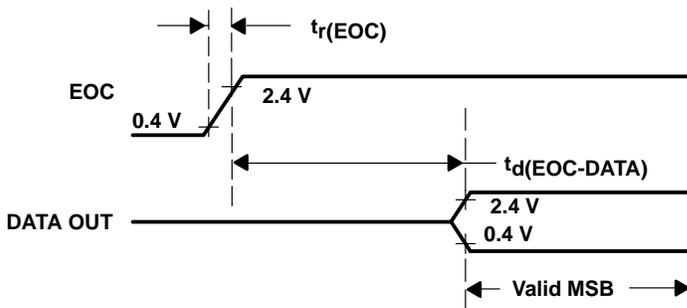   occurs while a conversion is ongoing.

Figure 5. $\overline{CS}$ and I/O CLOCK Voltage Waveforms
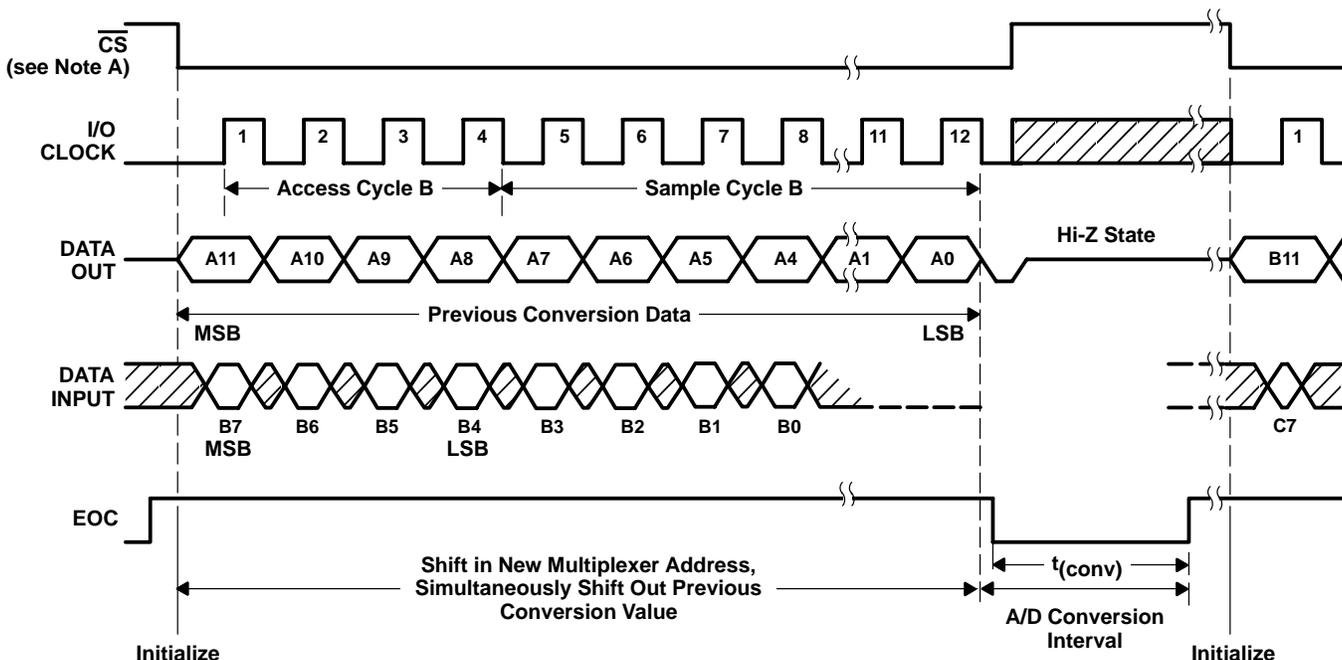
Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms
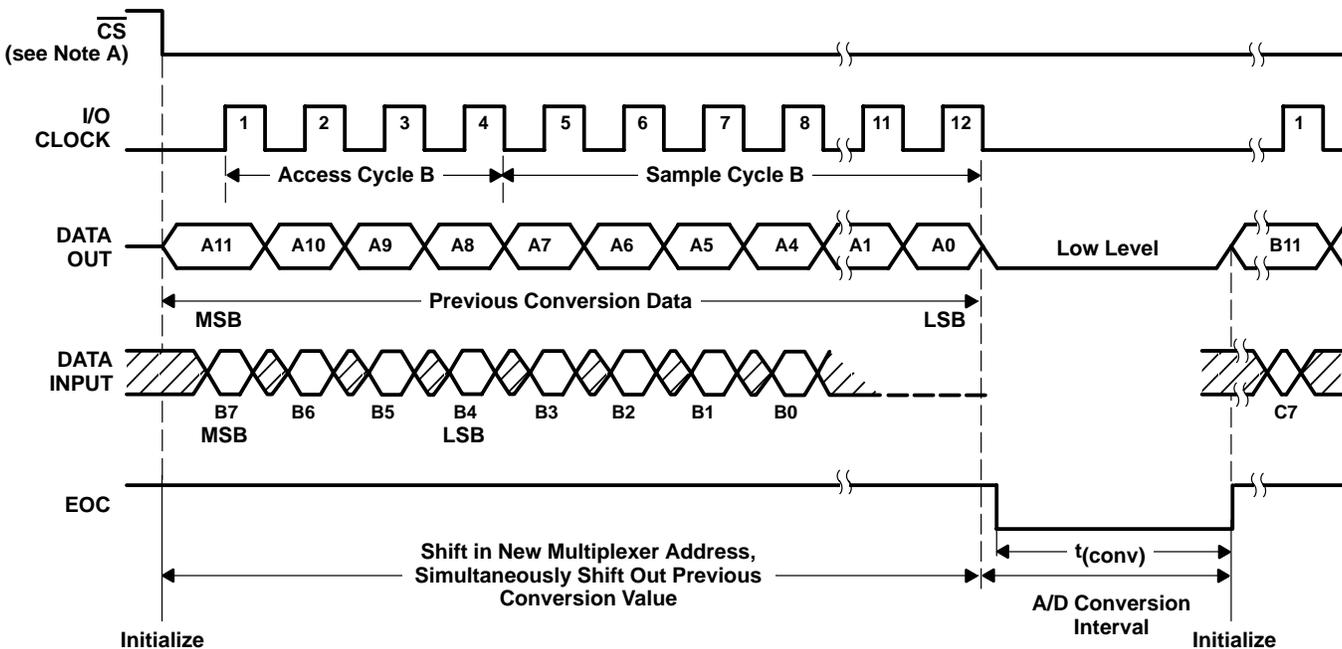
Figure 7. I/O CLOCK and EOC Voltage Waveforms

Figure 8. EOC and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

CS (see Note A)

I/O CLOCK

1 2 3 4 5 6 7 8 11 12 1

Access Cycle B — Sample Cycle B

DATA OUT

A11 A10 A9 A8 A7 A6 A5 A4 A1 A0 B11

Hi-Z State

Previous Conversion Data

MSB   LSB

DATA INPUT

B7 B6 B5 B4 B3 B2 B1 B0 C7
MSB   LSB

EOC

Shift in New Multiplexer Address, Simultaneously Shift Out Previous Conversion Value

$t_{(conv)}$

A/D Conversion Interval

Initialize   Initialize

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
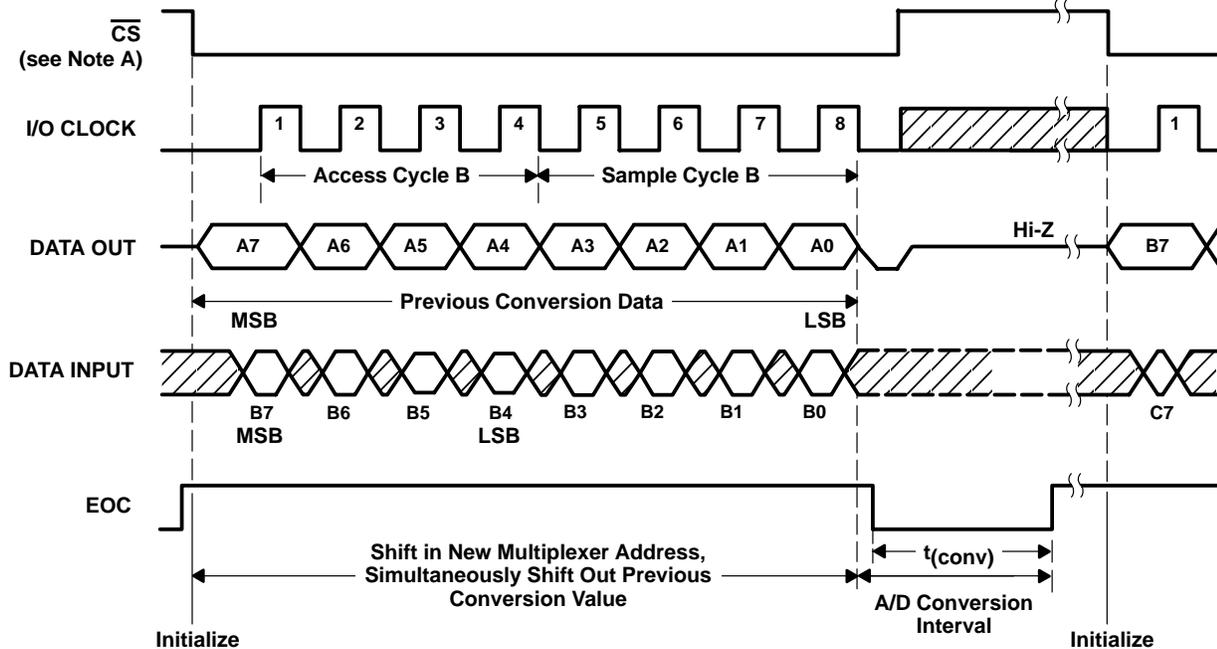
Figure 9. Timing for 12-Clock Transfer Using $\overline{CS}$ With MSB First

CS (see Note A)

I/O CLOCK

1 2 3 4 5 6 7 8 11 12 1

Access Cycle B — Sample Cycle B

DATA OUT

A11 A10 A9 A8 A7 A6 A5 A4 A1 A0 B11

Low Level

Previous Conversion Data

MSB   LSB

DATA INPUT

B7 B6 B5 B4 B3 B2 B1 B0 C7
MSB   LSB

EOC

Shift in New Multiplexer Address, Simultaneously Shift Out Previous Conversion Value

$t_{(conv)}$

A/D Conversion Interval

Initialize   Initialize

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
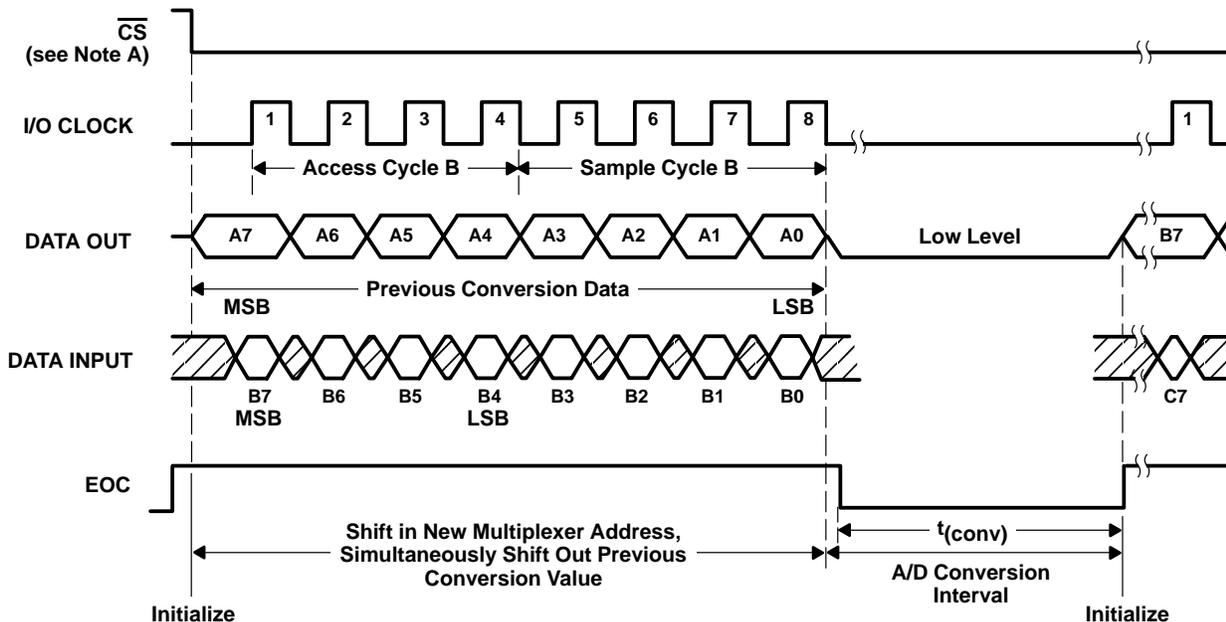
Figure 10. Timing for 12-Clock Transfer Not Using $\overline{CS}$ With MSB First

PARAMETER MEASUREMENT INFORMATION

CS (see Note A)

I/O CLOCK — 1 2 3 4 5 6 7 8 ... 1

Access Cycle B — Sample Cycle B

DATA OUT — A7 A6 A5 A4 A3 A2 A1 A0 — Hi-Z — B7

Previous Conversion Data

MSB — LSB

DATA INPUT — B7 B6 B5 B4 B3 B2 B1 B0 — C7

MSB — LSB

EOC

Shift in New Multiplexer Address, Simultaneously Shift Out Previous Conversion Value

t(conv)

A/D Conversion Interval

Initialize — Initialize

NOTE A: To minimize errors caused by noise at CS, the internal circuitry waits for a setup time after CS↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum CS setup time has elapsed.

Figure 11. Timing for 8-Clock Transfer Using CS With MSB First

CS (see Note A)

I/O CLOCK — 1 2 3 4 5 6 7 8 ... 1

Access Cycle B — Sample Cycle B

DATA OUT — A7 A6 A5 A4 A3 A2 A1 A0 — Low Level — B7

Previous Conversion Data

MSB — LSB

DATA INPUT — B7 B6 B5 B4 B3 B2 B1 B0 — C7

MSB — LSB

EOC

Shift in New Multiplexer Address, Simultaneously Shift Out Previous Conversion Value

t(conv)

A/D Conversion Interval

Initialize — Initialize

NOTE A: To minimize errors caused by noise at CS, the internal circuitry waits for a setup time after CS↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum CS setup time has elapsed.

Figure 12. Timing for 8-Clock Transfer Not Using CS With MSB First
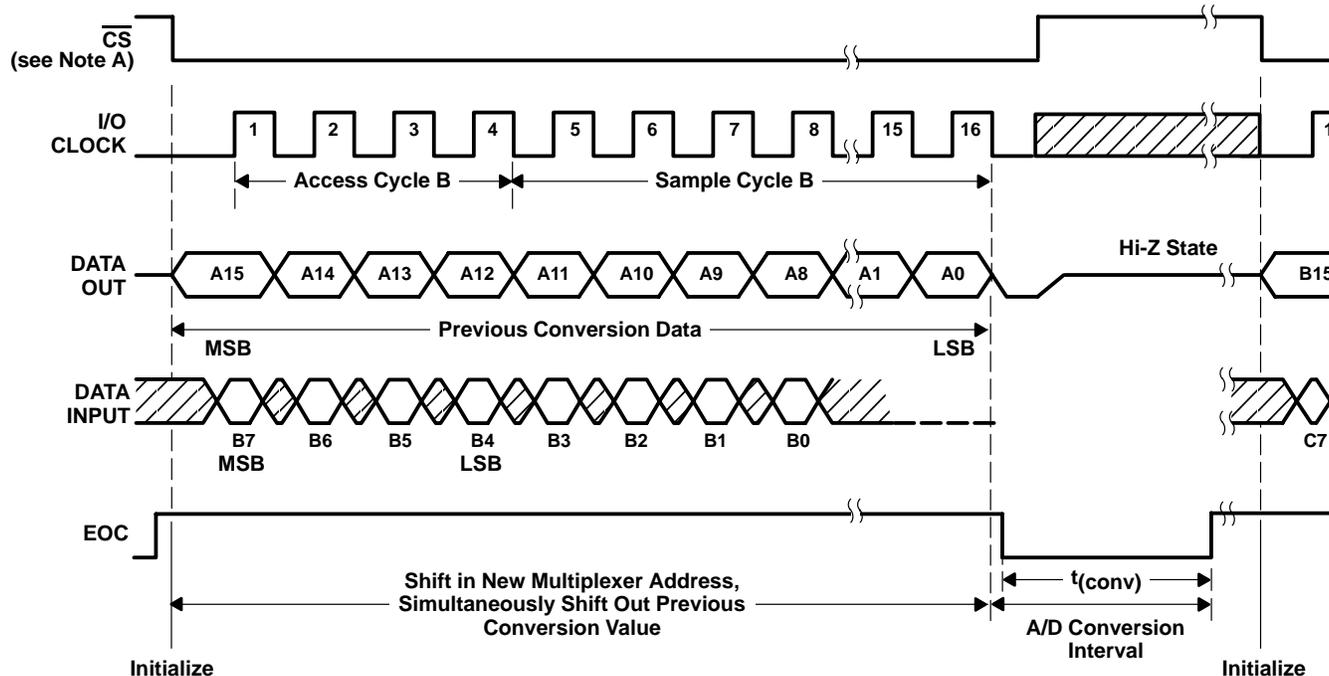
PARAMETER MEASUREMENT INFORMATION

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 13. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First
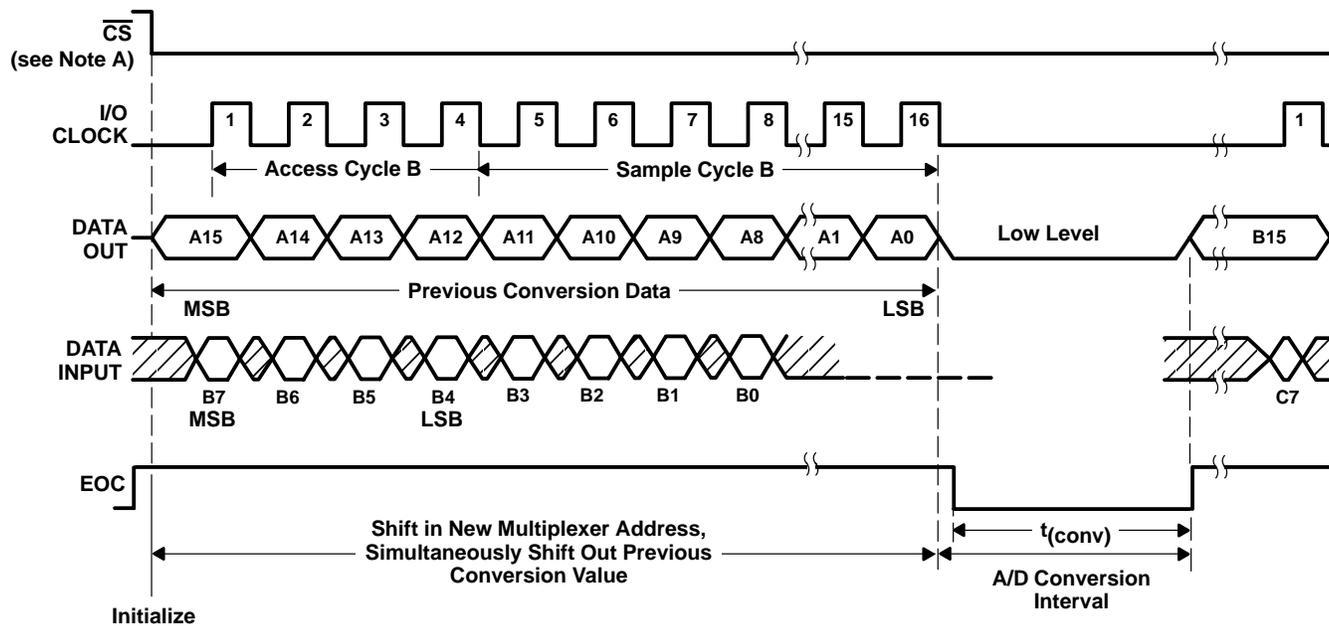
NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First

PRINCIPLES OF OPERATION

Initially, with chip select ($\overline{CS}$) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. $\overline{CS}$ going low begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7 – D4), a 2-bit data length select (D3 – D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clock cycles long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle and 2) the actual conversion cycle.

I/O cycle

The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

During the I/O cycle, the following two operations take place simultaneously.

An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12- or 16-clock I/O transfers.

The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. When $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. When $\overline{CS}$ is negated between conversions, the first output data bit occurs on the falling edge of $\overline{CS}$. This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

conversion cycle

The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

PRINCIPLES OF OPERATION

power up and initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and is then returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 1. Operational Terminology

Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion from DATA OUT
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle.
Previous (N−1) conversion cycle	The conversion cycle just prior to the current I/O cycle
Next (N+1) I/O cycle	The I/O period that follows the current conversion cycle

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even when this corrupts the output data from the previous conversion. The current conversion is begun immediately after the twelfth falling edge of the current I/O cycle.

PRINCIPLES OF OPERATION

data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 2 for the data input-register format).

Table 2. Input-Register Format

FUNCTION SELECT	INPUT DATA BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Select input channel								
AIN0	0	0	0	0				
AIN1	0	0	0	1				
AIN2	0	0	1	0				
AIN3	0	0	1	1				
AIN4	0	1	0	0				
AIN5	0	1	0	1				
AIN6	0	1	1	0				
AIN7	0	1	1	1				
AIN8	1	0	0	0				
AIN9	1	0	0	1				
AIN10	1	0	1	0				
Select test voltage								
$(V_{ref+} - V_{ref-})/2$	1	0	1	1				
V_{ref-}	1	1	0	0				
V_{ref+}	1	1	0	1				
Software power down	1	1	1	0				
Output data length								
8 bits					0	1		
12 bits					X†	0		
16 bits					1	1		
Output data format								
MSB first							0	
LSB first (LSBF)							1	
Unipolar (binary)								0
Bipolar (BIP) 2s complement								1

† X represents a do not care condition.

data input address bits

The four MSBs (D7 – D4) of the data register address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.

PRINCIPLES OF OPERATION

analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, then sampled and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 3. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	BINARY	HEX
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

Table 4. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED[†]	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX)[‡]
	BINARY	HEX	
$\dfrac{V_{ref+} - V_{ref-}}{2}$	1011	B	800
V_{ref-}	1100	C	000
V_{ref+}	1101	D	FFF

[†] V_{ref+} is the voltage applied to REF+, and V_{ref-} is the voltage applied to REF−.
[‡] The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Table 5. Power-Down-Select Address

| INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25\ \mu A$

PRINCIPLES OF OPERATION

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF−) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. When the voltage at the summing node is greater than the trip point of the threshold detector (approximately 1/2 V_{CC}), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF−. When the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

reference voltage inputs

The two reference inputs used with the device are the voltages applied to the REF+ and REF− terminals. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF− terminal voltage.
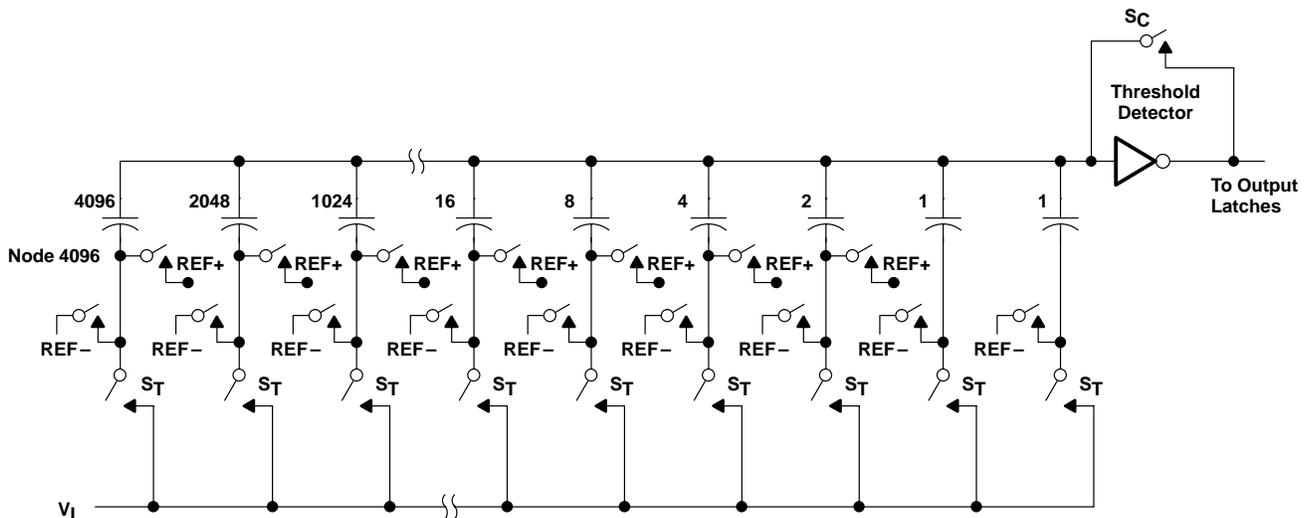
Figure 15. Simplified Model of the Successive-Approximation System

APPLICATION INFORMATION
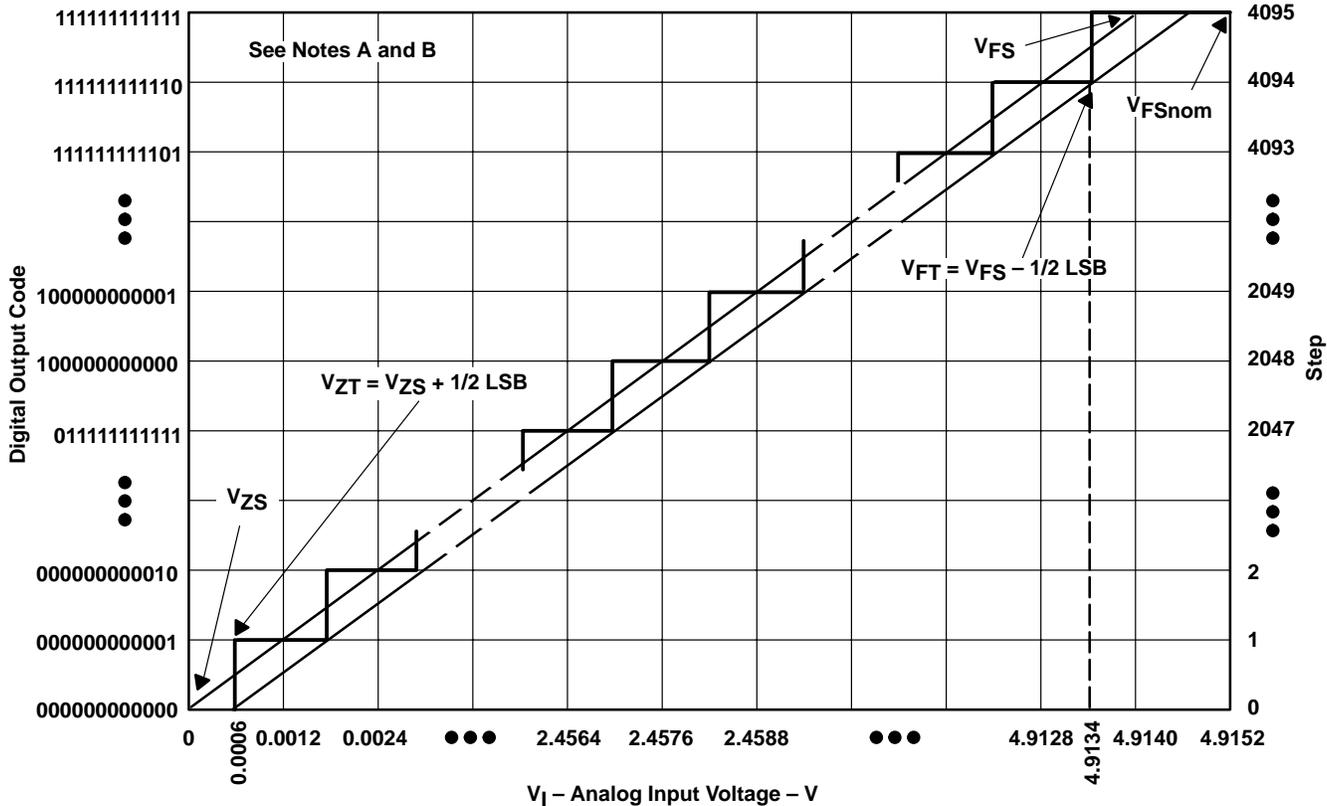
NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V and the transition to full scale (V_{FT}) is 4.9134 V. 1 LSB = 1.2 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 16. Ideal Conversion Characteristics
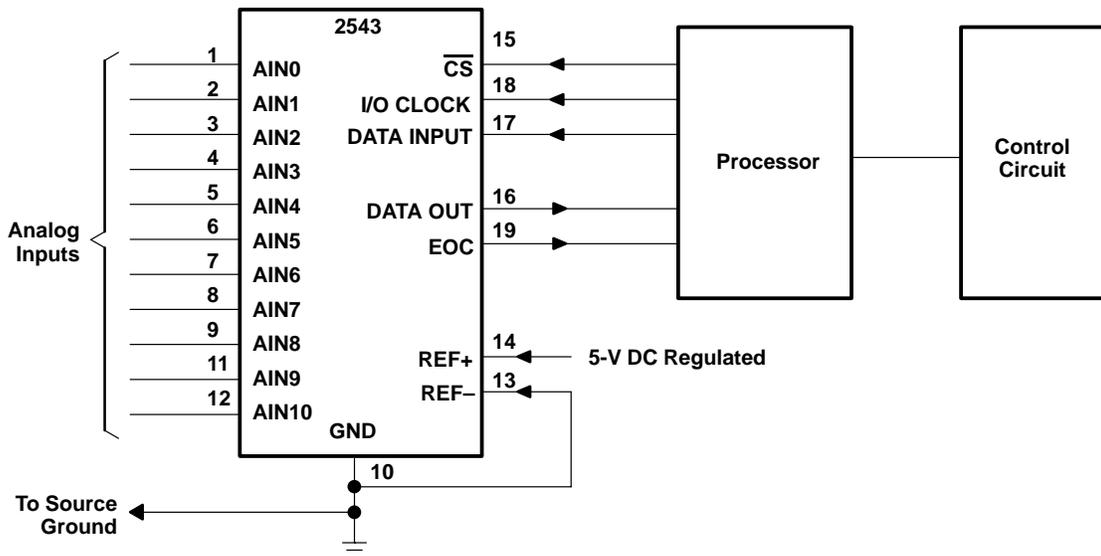
Figure 17. Serial Interface

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 18, the time required to charge the analog input capacitance from 0 V to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1 - e^{-t_C/R_t C_i}\right) \qquad (1)$$

Where:

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C \text{ (1/2 LSB)} = V_S - (V_S/8192) \qquad (2)$$

Equating equation 1 to equation 2 and solving for time t_C gives

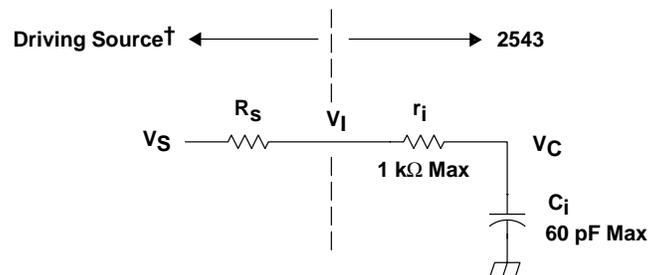$$V_S - \left(V_S/8192\right) = V_S\left(1 - e^{-t_C/R_t C_i}\right) \qquad (3)$$

and

$$t_C \text{ (1/2 LSB)} = R_t \times C_i \times \ln(8192) \qquad (4)$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_C \text{ (1/2 LSB)} = (R_S + 1\text{ k}\Omega) \times 60\text{ pF} \times \ln(8192) \qquad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.
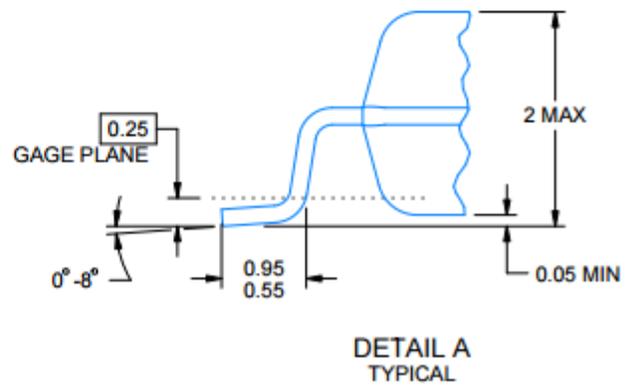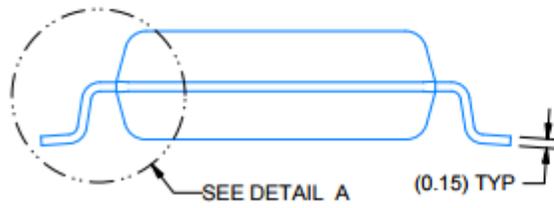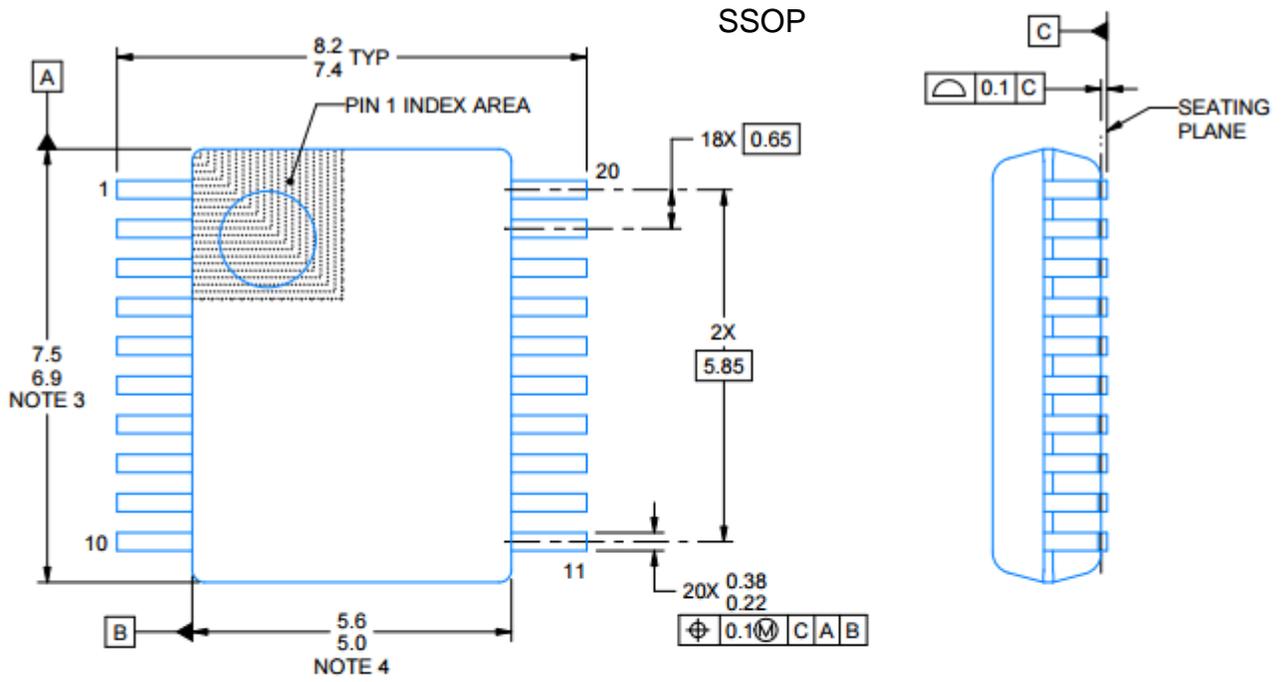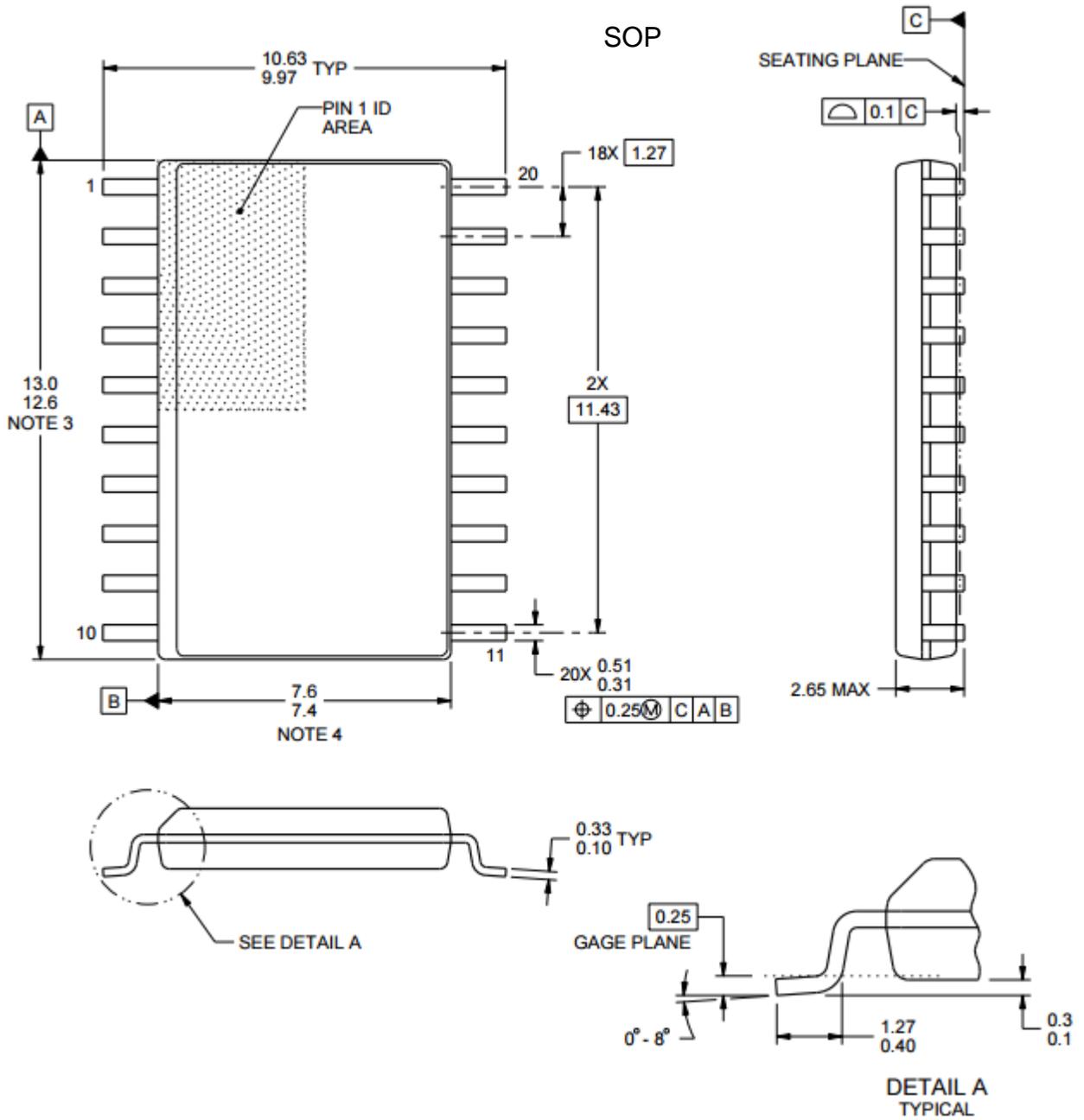

V_I = Input Voltage at AIN
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance
V_C = Capacitance Charging Voltage

† Driving source requirements:
 • Noise and distortion for the source must be equivalent to the resolution of the converter.
 • R_S must be real at the input frequency.

Figure 18. Equivalent Input Circuit Including the Driving Source

SSOP

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

20

18X 0.65

7.5 / 6.9
NOTE 3

2X 5.85

10

11

20X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

B

5.6 / 5.0
NOTE 4

C

△ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95 / 0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

SOP

SEATING PLANE

C

△ 0.1 C

10.63
9.97 TYP

A

PIN 1 ID
AREA

18X 1.27

1

20

13.0
12.6
NOTE 3

2X
11.43

10

11

7.6
7.4
NOTE 4

20X 0.51
0.31

⊕ 0.25Ⓜ C A B

2.65 MAX

B

SEE DETAIL A

0.33 TYP
0.10

0.25

GAGE PLANE

0°- 8°

1.27
0.40

0.3
0.1

DETAIL A
TYPICAL

尺寸 标注	最小(mm)	最大(mm)	尺寸 标注	最小(mm)	最大(mm)
A	26.43	26.63	D	7.74～8.0REF	
A1	2.44	2.64	D1	8.20	8.80
A2	0.41	0.51	D2	0.274TYP	
A3	1.524TYP		θ	6° TYP	
A4	1.073TYP		θ1	17° TYP4	
B	6.30	6.50	θ2	17° TYP4	
C	3.20	3.40	θ3	10° TYP4	
C1	1.48	1.58	θ4	10° TYP4	
C2	2.30	2.40	R	0.90TYP	
C3	3.20	3.40	φ	0.1±0.05TYP2	
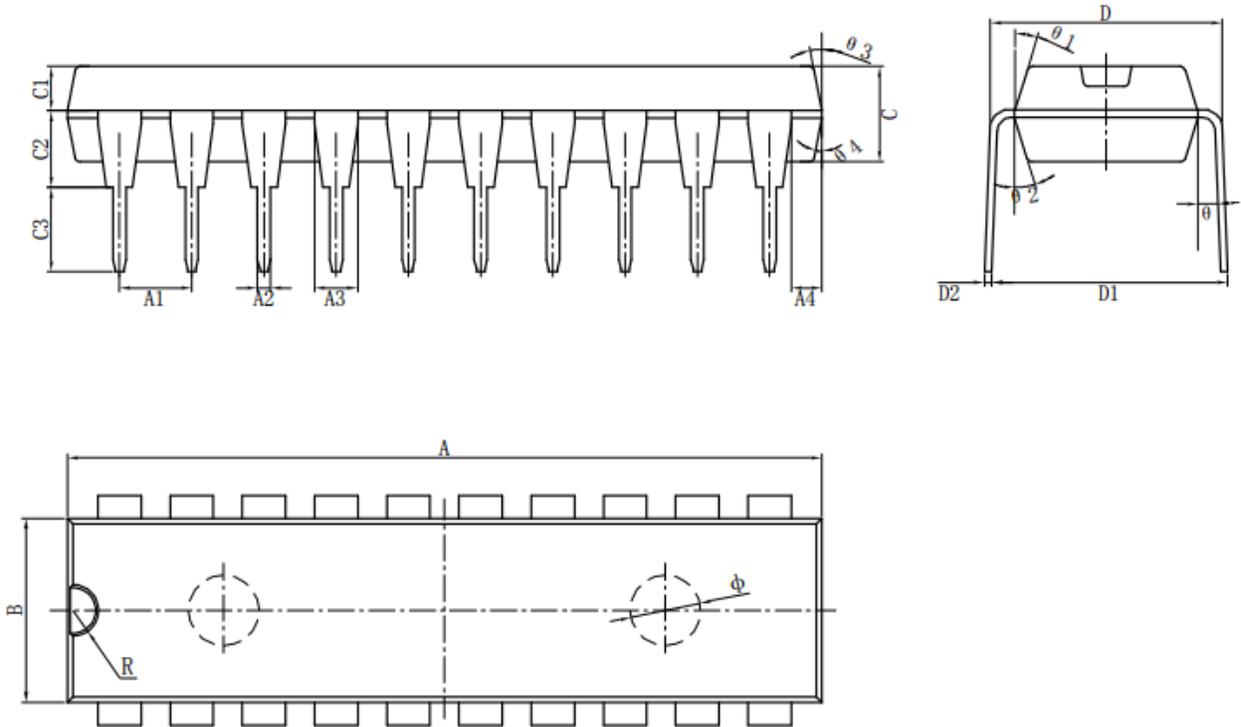
以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA