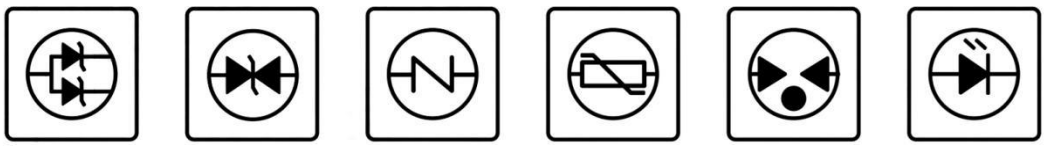
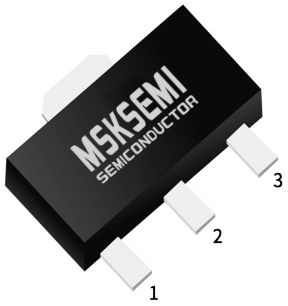
# MSKSEMI
SEMICONDUCTOR




# Product data sheet

www.msksemi.com




SOT-89

## FEATURES

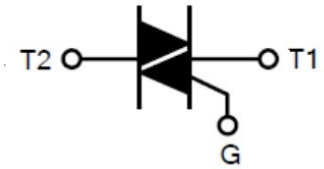
- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

## APPLICATIONS

- General purpose bidirectional switching
- General purpose low power phase control
- General purpose low power switching
- Solid-state relay

| Package | Pin assignment | | |
|---|---|---|---|
| | 1 | 2 | 3 |
| SOT-89 | T1 | T2 | G |

## SYMBOL:




## ABSOLUTE MAXIMUM RATINGS

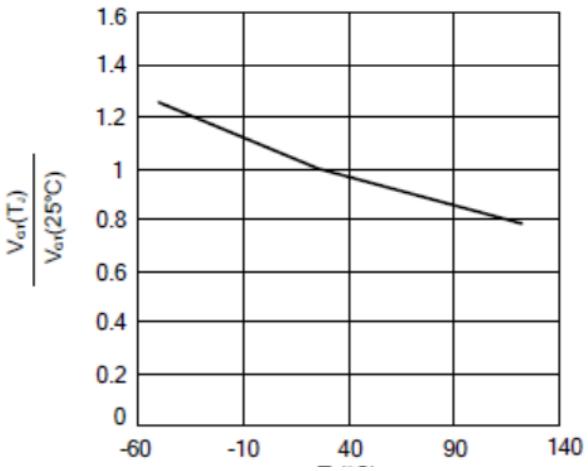
| PARAMETER | SYMBOL | VALUE | | UNIT |
|---|---|---|---|---|
| Repetitive Peak Off-State Voltages | $V_{DRM}$, $V_{RRM}$ | MAC97A6 | 400 | V |
| | | MAC97A8 | 600 | |
| RMS on-State Current | $I_{T(RMS)}$ | 0.8 | | A |
| Non-Repetitive Peak On-State Current | $I_{TSM}$ | 8 | | A |
| $I^2t$ for fusing | $I^2t$ | 0.32 | | $A^2s$ |
| Repetitive rate of rise of on-state current after triggering | dIT/dt | I | 50 | A/uS |
| | | II | 50 | |
| | | III | 50 | |
| | | IV | 10 | |
| Peak gate current | $I_{GM}$ | 1 | | A |
| Peak Gate Voltage | $V_{GM}$ | 5 | | V |
| Peak Gate Power | $P_{GM}$ | 5 | | W |
| Average Gate Power | $P_{G(AV)}$ | 0.1 | | W |
| Operating junction temperature | $T_J$ | +125 | | ℃ |
| Storage Temperature | $T_{STG}$ | -40 ~ +150 | | ℃ |

## ELECTRICAL CHARACTERISTICS (TJ=25°C)

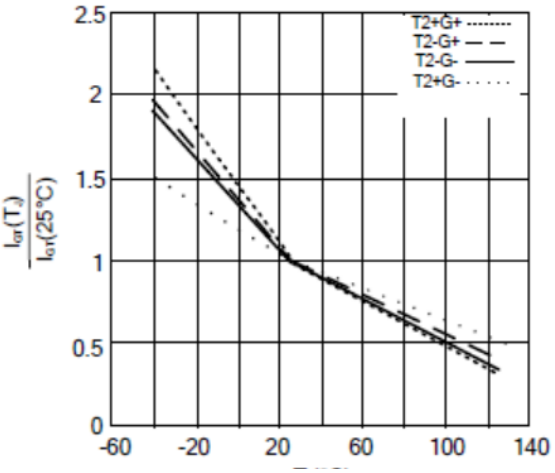
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|
| Peak Repetitive Forward or Reverse Blocking Current | $I_{DRM}$ $I_{RRM}$ | $V_{AK}$ = Rated $V_{DRM}$ or $V_{RRM}$; | | | 10 | uA |
| Gate Trigger Current | $I_{GT}$ | $V_D$=12V $I_{GT}$=0.1A | I | | 5.0 | mA |
| | | | II | | 5.0 | |
| | | | III | | 5.0 | |
| | | | IV | | 7.0 | |
| Gate Trigger Voltage | $V_{GT}$ | $V_D$=12V, RL=100Ω | | | 2.0 | V |
| Peak Forward On-State Voltage | $V_{TM}$ | IT=1.0A, | | | 1.7 | V |
| Holding Current | $I_L$ | $V_D$=12V $I_G$=0.1A, | I | | 10 | mA |
| | | | II | | 20 | |
| | | | III | | 10 | |
| | | | IV | | 10 | |
| Latch Current | $I_H$ | $V_D$=12V ,IG=0.1A | | | 10 | mA |
| Critical Rate of Rise of Off-State Voltage | dV/dt | $V_D$=67%$V_{DRM}$, $R_{GK}$=1kΩ, | | 10 | | V/μs |

## ELECTRICAL CHARACTERISTIC CURVE

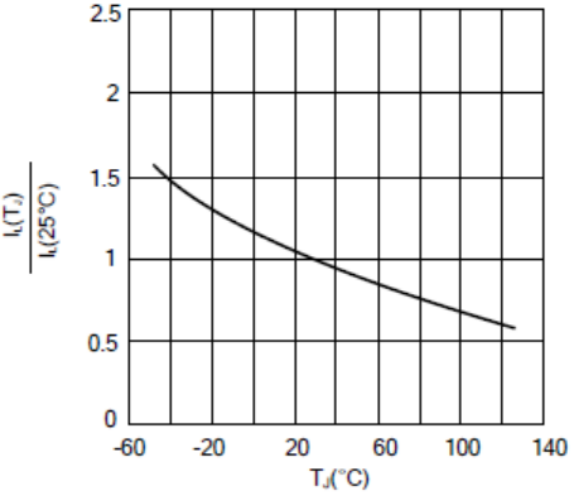
Normalized Gate Trigger Voltage as a of Function Junction Temperature; Typical Values.



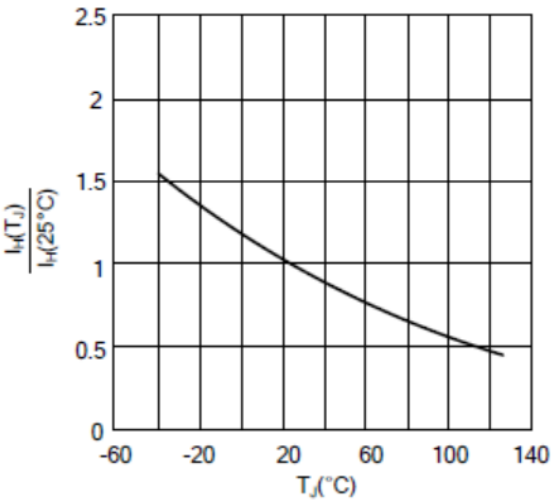

Normalized Gate Trigger Current as a Function of Junction Temperature; Typical Values.



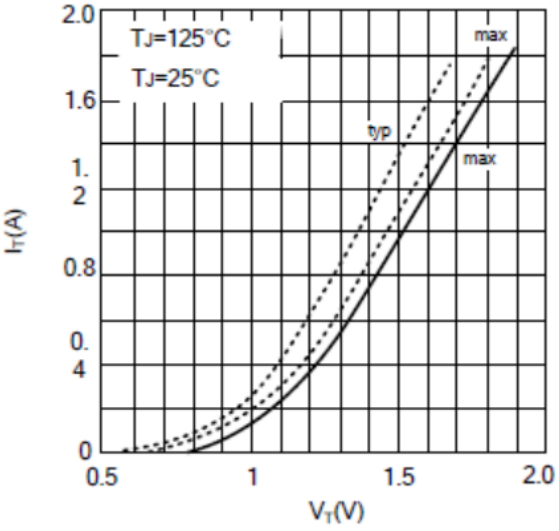
Normalized Latching Current as a Function of Junction Temperature; Typical Values.



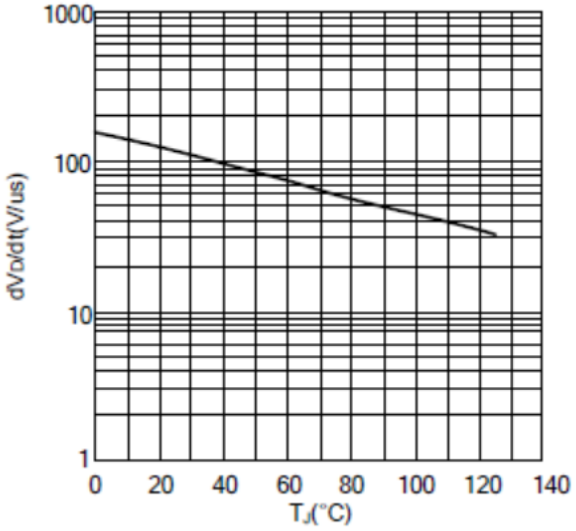

Normalized Holding Current as a Function of Junction Temperature; Typical Values.



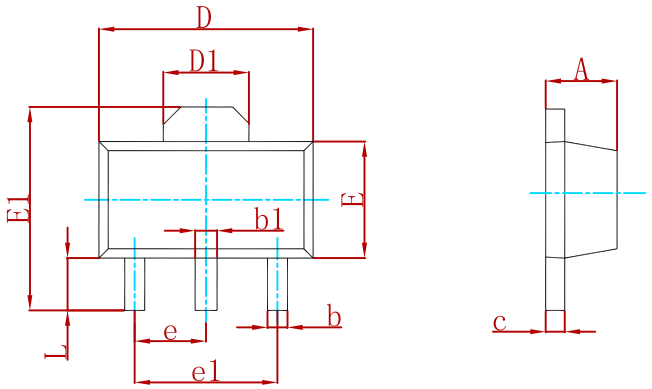

On-State Current as a Function of On-State Voltage; Typical and Maximum Values.




Critical Rate of Rise of Off-State Voltage as a Function of Junction Temperature; Typical Values.

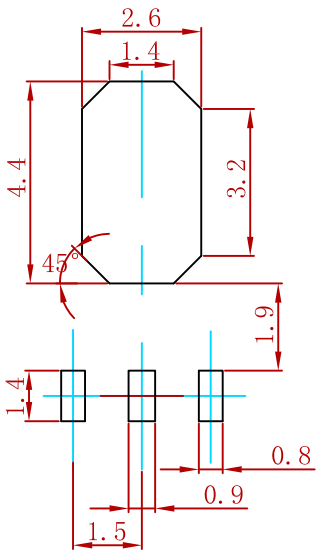


## PACKAGE MECHANICAL DATA




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.400 | 1.600 | 0.055 | 0.063 |
| b | 0.320 | 0.520 | 0.013 | 0.020 |
| b1 | 0.400 | 0.580 | 0.016 | 0.023 |
| c | 0.350 | 0.440 | 0.014 | 0.017 |
| D | 4.400 | 4.600 | 0.173 | 0.181 |
| D1 | 1.550 REF. | | 0.061 REF. | |
| E | 2.300 | 2.600 | 0.091 | 0.102 |
| E1 | 3.940 | 4.250 | 0.155 | 0.167 |
| e | 1.500 TYP. | | 0.060 TYP. | |
| e1 | 3.000 TYP. | | 0.118 TYP. | |
| L | 0.900 | 1.200 | 0.035 | 0.047 |

## Suggested Pad Layout




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

## REEL SPECIFICATION

| P/N | PKG | QTY |
|---|---|---|
| MAC97A6 THRU MAC97A8 | SOT-89 | 1000 |

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