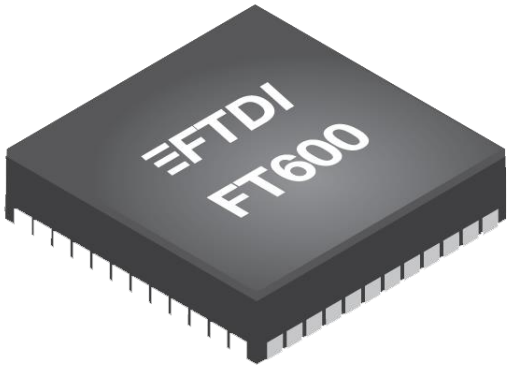
Future Technology Devices International Ltd.

FT600Q-FT601Q IC Datasheet

(USB 3.0 to FIFO Bridge)



The FT600/FT601 is a USB 3.0 to FIFO interface bridge chip with the following advanced features:

- Supports USB 3.0 Super Speed (5Gbps)/USB 2.0 High Speed (480Mbps)/USB 2.0 Full Speed (12Mbps) transfer.
- Supported USB Transfer Type: Control/Bulk/Interrupt
- Up to 8 configurable endpoints (PIPEs).
- Supports 2 parallel slave FIFO bus protocols 245 and FIFO mode, FT601 with 32 bit parallel interface has a data bursting rate up to 400MB/s.
- Supports 4 IN channels and 4 OUT channels on FIFO bus connectivity.
- Built-in 16kB FIFO data buffer RAM.
- Supports Remote Wakeup capability.
- Supports multi voltage I/O: 1.8V, 2.5V and 3.3V.
- Configurable GPIO support.
- Internal LDO 1.0V regulator.
- Integrated power-on-reset circuit.
- User programmable USB descriptors.
- Supports Battery Charging spec. BC1.2 battery charging detection.
- Available as FT600-16bit/FT601-32bit FIFO interface.
- Industrial operating temperature range: -40 to 85^0C.
- Available in compact Pb-free QFN-76(32bit) and QFN-56(16bit) packages (both RoHS compliant).

1 Typical Applications

- Upgrading Legacy Peripherals to USB
- Utilising USB to add system modularity
- Interfacing PLD/FPGA based designs to USB 3.0
- USB 3.0 data acquisition
- USB 3.0 Digital Video Camera Interface
- USB 3.0 Digital Camera
- USB 3.0 Interface for Printer/Scanner
- Medical/Industrial imaging devices
- USB 3.0 Instrumentation

1.1 Driver Support

Royalty free D3XX *Direct* Drivers
(USB Drivers + DLL S/W Interface)

- Windows 10
- Windows 8
- Windows 7
- Mac OS-X (available in 2017)
- Linux

The drivers listed above are all available to download for free from the FTDI website (www.ftdichip.com). For driver installation, please refer to http://www.ftdichip.com/Drivers/D3XX.htm

1.2 Ordering Information

Part Number	Package	Remark
FT600Q-B-x	56 Pin QFN 0.4mm Pitch	Rev B
FT601Q-B-x	76 Pin QFN 0.4mm Pitch	Rev B

Table 1.1 Device Part Numbers

Note: Packaging codes for x is:

-R: Taped and Reel, (VQFN in 3000 pieces per reel)

-T: Tray packing, (VQFN in 260 pieces per tray)

For example: FT600Q-B-R is 3000 QFN pieces in taped and reel packaging (rev B)

1.3 USB Compliant

Both FT600 and FT601 are fully compliant with the USB 3.1 specification for Generation 1 devices. USB IF TID 340930018 applies to the FT600 and TID 340930019 for the FT601.

2 Block Diagram

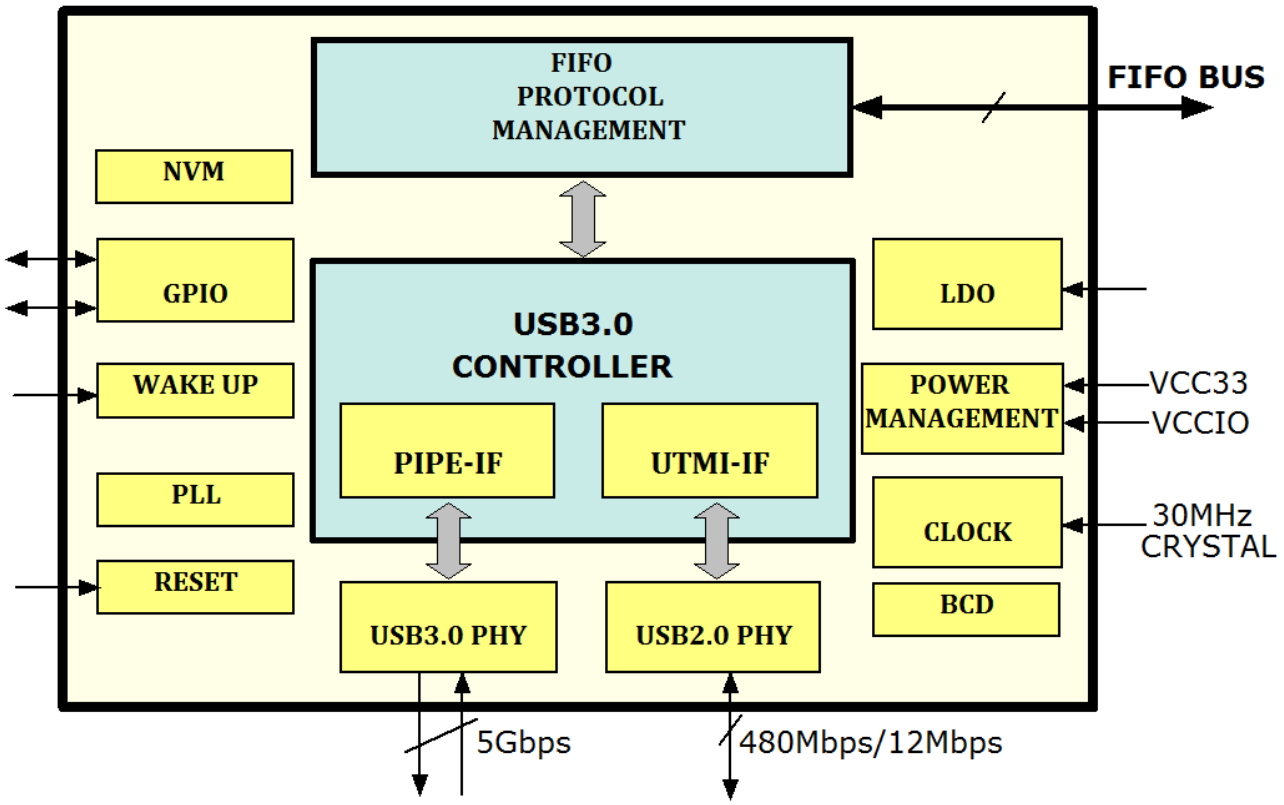


Figure 2.1 Block Diagram

Notes: FT600Q(QFN-56) has a 16-bit FIFO bus interface and FT601Q(QFN-76) has a 32-bit FIFO bus interface.

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 Device Pin Out

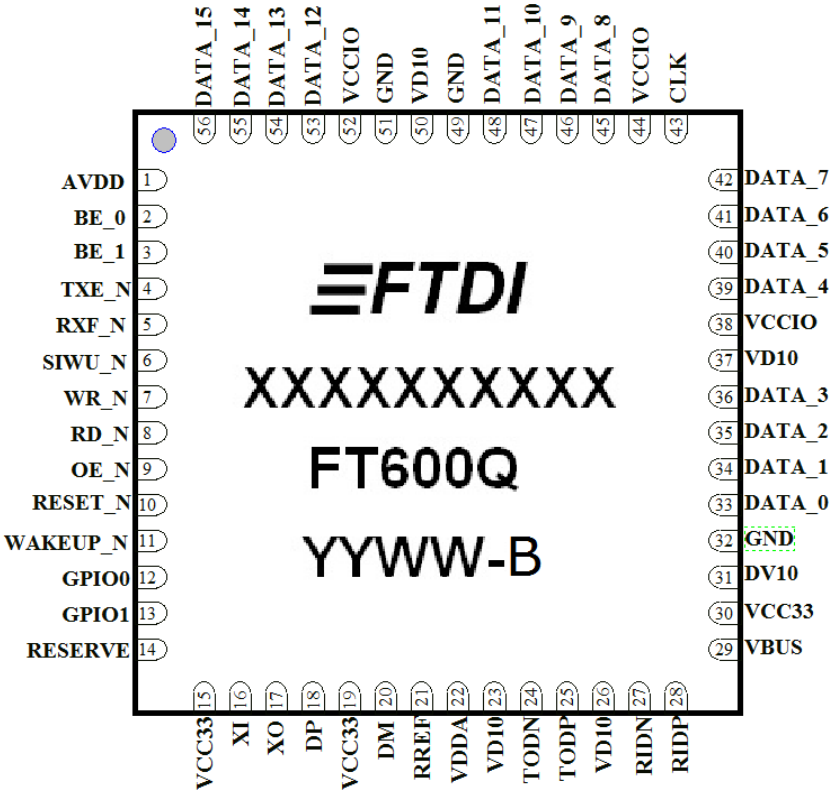


Figure 3.1 QFN56 Package Pin Out

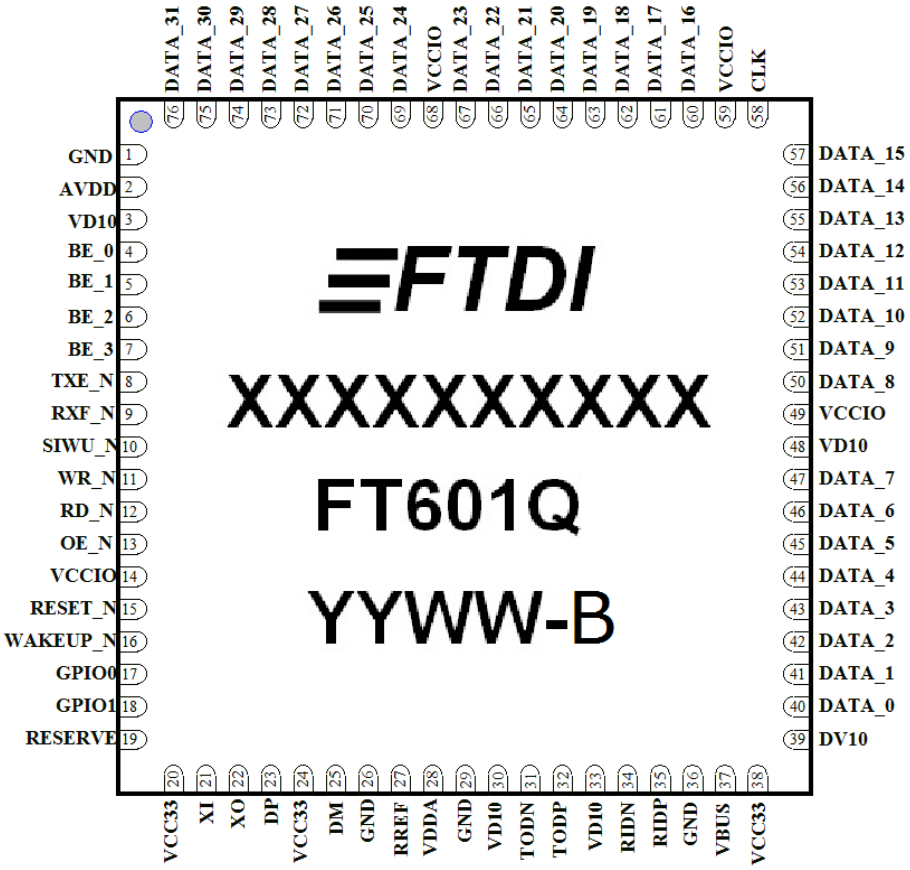


Figure 3.2 QFN76 Package Pin Out

3.2 Device Pin Out Signal Description

Pin Name	Description	Type	Pin No.	
			QFN76	QFN56
CLK	Parallel FIFO bus clock output pin to FIFO bus master, the Frequency can be configured as 66Mhz or 100Mhz for both FIFO bus modes.	O	58	43
DATA_0	Parallel FIFO bus data I/O bit 0.	I/O	40	33
DATA_1	Parallel FIFO bus data I/O bit 1.	I/O	41	34
DATA_2	Parallel FIFO bus data I/O bit 2.	I/O	42	35
DATA_3	Parallel FIFO bus data I/O bit 3.	I/O	43	36
DATA_4	Parallel FIFO bus data I/O bit 4.	I/O	44	39
DATA_5	Parallel FIFO bus data I/O bit 5.	I/O	45	40
DATA_6	Parallel FIFO bus data I/O bit 6.	I/O	46	41
DATA_7	Parallel FIFO bus data I/O bit 7.	I/O	47	42
DATA_8	Parallel FIFO bus data I/O bit 8.	I/O	50	45

DATA_9	Parallel FIFO bus data I/O bit 9.	I/O	51	46
DATA_10	Parallel FIFO bus data I/O bit 10.	I/O	52	47
DATA_11	Parallel FIFO bus data I/O bit 11.	I/O	53	48
DATA_12	Parallel FIFO bus data I/O bit 12.	I/O	54	53
DATA_13	Parallel FIFO bus data I/O bit 13.	I/O	55	54
DATA_14	Parallel FIFO bus data I/O bit 14.	I/O	56	55
DATA_15	Parallel FIFO bus data I/O bit 15.	I/O	57	56
DATA_16	Parallel FIFO bus data I/O bit 16.	I/O	60	N/A
DATA_17	Parallel FIFO bus data I/O bit 17.	I/O	61	N/A
DATA_18	Parallel FIFO bus data I/O bit 18.	I/O	62	N/A
DATA_19	Parallel FIFO bus data I/O bit 19.	I/O	63	N/A
DATA_20	Parallel FIFO bus data I/O bit 20.	I/O	64	N/A
DATA_21	Parallel FIFO bus data I/O bit 21.	I/O	65	N/A
DATA_22	Parallel FIFO bus data I/O bit 22.	I/O	66	N/A
DATA_23	Parallel FIFO bus data I/O bit 23.	I/O	67	N/A
DATA_24	Parallel FIFO bus data I/O bit 24.	I/O	69	N/A
DATA_25	Parallel FIFO bus data I/O bit 25.	I/O	70	N/A
DATA_26	Parallel FIFO bus data I/O bit 26.	I/O	71	N/A
DATA_27	Parallel FIFO bus data I/O bit 27.	I/O	72	N/A
DATA_28	Parallel FIFO bus data I/O bit 28.	I/O	73	N/A
DATA_29	Parallel FIFO bus data I/O bit 29.	I/O	74	N/A
DATA_30	Parallel FIFO bus data I/O bit 30.	I/O	75	N/A
DATA_31	Parallel FIFO bus data I/O bit 31.	I/O	76	N/A
BE_0	Parallel FIFO bus byte enable I/O bit 0.	I/O	4	2
BE_1	Parallel FIFO bus byte enable I/O bit 1.	I/O	5	3
BE_2	Parallel FIFO bus byte enable I/O bit 2.	I/O	6	N/A
BE_3	Parallel FIFO bus byte enable I/O bit 3.	I/O	7	N/A
TXE_N	245 Synchronous FIFO mode: Transmit FIFO Empty output signal. The signal indicates there is a minimum of 1 byte of space available to write to. Only write to the FIFO when	O	8	4

	this signal is logic 0. Multi-Channel FIFO mode: Status Valid output signal (optional).			
RXF_N	245 Synchronous FIFO mode: Receive FIFO Full output signal. The signal indicates there is a minimum of 1 byte of data available to read. Only read from the FIFO when this signal is logic 0. Multi-Channel FIFO mode: Data Receive Acknowledge output signal.	O	9	5
SIWU_N	Reserved. Add external pull up in normal operation.	I	10	6
WR_N	245 Synchronous FIFO mode: Write Enable input signal. Multi-Channel FIFO mode: Data Transaction Request input signal. The signal is active low.	I	11	7
RD_N	245 Synchronous FIFO mode: Read Enable input signal. The signal is active low.	I	12	8
OE_N	245 Synchronous FIFO mode: Data Output Enable input signal. The signal is active low.	I	13	9
RESET_N	Chip Reset input, Active low.	I	15	10
WAKEUP_N	Suspend/Remote Wakeup pin by default Low when USB is active, high when USB is in suspend. Application can drive this pin low in in USB suspend to generate a remote wakeup signal to the USB host.	I/O	16	11
Reserved	Do not connect.	NC	19	14
GPIO0	Configurable GPIO port0.	I/O	17	12
GPIO1	Configurable GPIO port1.	I/O	18	13
VBUS	USB BUS power input.	I	37	29
XI	Crystal input. This terminal is the crystal input for the internal oscillator.	I	21	16
XO	Crystal Output. This terminal is the crystal output for the internal oscillator.	O	22	17
DP	High-speed USB differential transceiver (positive)	I/O	23	18
DM	High-speed USB differential transceiver (negative)	I/O	25	20

RREF	PHY reference resistor input pin. Connect 1.6K Ω 1% resistor to ground, provides reference voltage to USB2 PHY.	I	27	21
TODN	Super Speed USB transmitter differential pair (negative)	O	31	24
TODP	Super Speed USB transmitter differential pair (positive)	O	32	25
RIDN	Super Speed USB receiver differential pair (negative)	I	34	27
RIDP	Super Speed USB receiver differential pair (positive)	I	35	28
VCC33	+3.3V power input for chip and internal LDO.	PWR	20,24, 38	15,19, 30
DV10	+1.0V power output from internal LDO. Connecting to VD10 and AVDD, with a 4.7uF cap to ground is recommended.	O	39	31
VD10	+1.0V core voltage input.	PWR	3,30,3 3,48	23,26, 37,50
VCCIO	Power input for I/O block, supports +1.8/+2.5/+3.3V.	PWR	14,49, 59,68	38,44, 52
VDDA	+3.3V power input for USB2.0 and USB3.0 PHYs.	PWR	28	22
AVDD	+1.0V power input for PLL.	PWR	2	1
GND	Ground	GND	1,26, 29,36	32, 49,51

Table 3.1 Device pin out Signal descriptions

4 Function Description

FT60x is a high performance USB 3.0-to-FIFO interface bridge chip. This device can be used in those applications which require high data throughput such as imaging devices and Multi-Channel FIFO ADC or DAC devices etc.

The FIFO interface can support multi-voltage I/O (1.8V, 2.5V, 3.3V) and operating frequencies of 66.67MHz or 100MHz. 100MHz only for 2.5V and 3.3V.

There are 2 different proprietary synchronous bus protocols supported; one FIFO bus protocol is called the "Multi-Channel FIFO" bus protocol and the other is the "245 Synchronous FIFO" bus protocol. The latter being an extension of the interface introduced in the FT232H/FT2232H devices.

4.1 Key Features and Function Description

Functional Integration

The following features are integral to the IC design: FIFO protocol management, USB 3.0 controller, USB3.0 and USB2.0 PHYs, GPIOs, power management, clock generation, power-on-reset (POR) and LDO regulator.

USB 3.0 Protocol Controller

The USB 3.0 Protocol Controller manages the data stream from the device USB control endpoint. It handles the USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the FIFO in accordance with the USB 3.0 specification.

FIFO Management

This unit is used to manage all PIPE data or buffers in the FIFO memory; the data is sent or received through the FIFO protocol layer. Through this block the FIFO memory can be allocated to each PIPE with any size of memory as long as the total memory allocated to all PIPEs does not exceed the maximum FIFO memory size which is 16KB. Additionally, the FIFO signals have a configurable high drive strength capability and can be set to 18Ω, 25Ω, 35Ω and 50Ω.

Multi-Channel FIFO Bus protocol

The multi-Channel FIFO bus is a slave bus and is designed to handle Multi-Channel FIFO connectivity. The bus protocol supports a total of 8 channels (4 INs and 4 OUTs). CLK is the clock output to the FIFO bus master.

245 Synchronous FIFO Bus protocol

The 245 Synchronous FIFO bus is a slave bus with one IN and one OUT FIFO channel supported by this bus protocol. CLK is the clock output to the FIFO bus master.

FIFO Bus Clock Option

The device provides the following FIFO bus clock frequency option: 100MHz.

FIFO RX/TX Buffer (16k bytes)

Data sent from the USB host controller to the FIFO via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer and is removed from the buffer by reading the contents of the FIFO using the RD# pin. (RX relative to the USB interface).

Data written into the FIFO using the WR pin is stored in the FIFO TX (transmit) Buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (TX relative to the USB interface).

When the FT600 or FT601 is configured as the 245 Synchronous FIFO bus or 1 channel in the multi-Channel FIFO bus mode, the FIFO buffer is configured as 4 KB * 2 (double buffered) each on the RX and TX channels.

When the FT600 or FT601 is configured as 2 channels in the multi-Channel FIFO bus mode, the FIFO buffer is configured as 2 KB * 2 (double buffered) each on RX and TX channel.

When the FT600 or FT601 is configured as 4 channels in the multi-Channel FIFO bus mode, the FIFO buffer is configured as 1 KB * 2 (double buffered) each on RX and TX channel.

Internal LDO Regulator

The LDO regulator generates the +1.0V power supply for driving the internal core of the device. Not to be used for external devices.

Reset Generator

The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET_N input pin allows an external device to reset the FT60x. Active low.

Remote Wake Up Function

If USB is in suspend mode, and remote wake up has been enabled, driving the WAKEUP_N pin to low will cause the FT60x device to request a resume from suspend on the USB bus. Normally this can be used to wake up the host PC from suspend.

BCD(Battery Charge Detection) Function

Supports Battery Charging spec revision 1.2, it is optional for mapping the GPIO pin to indicate the detect results. Refer to GPIO for the pin configuration in BCD mode.

GPIO (General purpose input and output) pins

GPOI[1:0] are multifunctional pins. The functions are configured by the chip configuration data. The default chip configuration sets the GPIO pins as FIFO mode configuration input. At the power up, FT600 or FT601 sets the chip to 245 synchronous FIFO mode or multi-channel FIFO modes depending on the GPIO[1:0] input, details in the table below:

GPIO1	GPIO0	Chip mode
0	0	1 channel, 245 Synchronous FIFO mode
0	1	1 channel, Multi-Channel FIFO mode
1	0	2 channel, Multi-Channel FIFO mode
1	1	4 channel, Multi-Channel FIFO mode

To enable the GPIO function, the chip configuration must be updated to set the GPIO function.

To enable the BCD mode, the chip configuration must be updated to set the BCD mode.

When the FT600 or FT601 is configured to support BCD, the GPIO pins are set to output, output changes according to BCD detection result.

GPIO1	GPIO0	Chip mode
0	0	No USB connection or BCD detection on going.
0	1	SDP(standard downstream port) detected
1	0	CDP(Charging downstream port) detected
1	1	DCP(Dedicated charging port) detected

4.2 Multi-Channel FIFO Mode Protocols

This is a Slave bus and is designed to handle multi-channel connectivity. The bus protocol supports a total of 4 bidirectional channels; each has 1 USB OUT and 1 USB IN endpoints. . CLK is the clock output from the bus slave to the bus master.

The channel number denoted in this document as channel 1 to 3 mapped to USB endpoint number 2 to 5. The USB OUT endpoint in Channel 1 is denoted as USB out channel 1, USB IN endpoint in channel 1 is denoted as USB IN channel 1.

Correspondingly, the FIFO OUT is for data transmitted from USB host to device and FIFO IN is for data transmitted from USB device to host.

WR_N is the bus master to bus slave data transaction request signal, and it is active low.

RXF_N is the bus slave to bus master data receive acknowledge signal, and it is active low.

TXE_N (optional signal, master can ignore this signal) is the bus slave to bus master FIFO idle status valid signal, and it is low active.

DATA[31:0] is used as the 32-bit data bus during the data transfer phase. When the bus is in the idle state DATA[31:16], DATA[7:0] and BE[3:0] are driven to logic"1" by the bus master, and DATA[15:8] is driven by the bus slave to provide the FIFO status to the bus master. The upper nibble (DATA[15:12]) provides the 4 OUT channels FIFO status while the lower nibble (DATA[11:8]) provides the 4 IN channels FIFO status. They are all active low.

For example, at idle, DATA[12] is logic"0" and DATA[8] is logic"0", which indicates USB OUT channel 1 FIFO data is available to send and USB IN channel 1 FIFO space is empty to receive data respectively. The external bus master will start a transfer cycle by asserting WR_N based on the channel FIFO status. The first cycle after WR_N is asserted is the command phase, followed by the data phase when RXF_N is asserted. At the command phase, the bus master will send the channel number which it intends to transfer data with on DATA[7:0] and the Read/Write command on BE[3:0]. BE[3:0] = 'h0 and BE[3:0] = 'h1 indicates a master read or write respectively. There may also be a required turn-a-round for DATA[31:0] and BE[3:0] after the command phase and at the end of data transaction. BE[1:0] is valid for FT600 2 byte wide data interface.

Table 4.1 shows Multi-Channel FIFO mode command phase master read/write and channel address setting.

Command Phase	FT600 Command BE[1:0]	FT601 Command BE[3:0]	Channel Address DATA[7:0]
Master Read	00	0000	8'h1=Channel 1 8'h2=Channel 2 8'h3=Channel 3 8'h4=Channel 4
Master Write	01	0001	

Table 4.1 Multi-Channel FIFO mode Command phase

The waveform below shows a FT601 master read transaction of 10 bytes with FIFO data exhausted first at channel 1. There are turn-a-round cycles for DATA[7:0], DATA[31:16] and BE[3:0] after command phase and at the end of the data transaction. The BE[3:0] shows that the lower 2 bytes in D2 are valid at the last word strobe in this transaction.

In this waveform, there are 2 bus turn around cycles 1 and 2. The FIFO master releases the bus in bus turns around 1, after which, the FT601 asserts the RXF_N indicating it drives valid data on the bus. The FT601 releases the bus on bus turn around 2, the FIFO master should sample the FIFO status after the bus turn around 2.

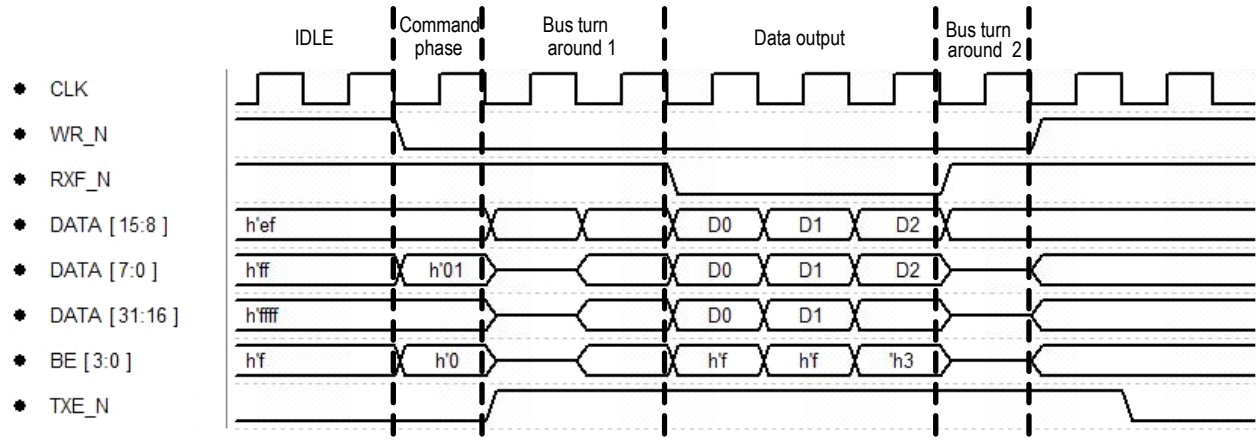


Figure 4.1 FT601 Multi-Channel FIFO mode master read transaction 1

The waveform below shows a FT601 master read transaction for 12 valid bytes at channel 1, where the bus master terminates the transaction. There are turn-a-round cycles for DATA[7:0], DATA[31:16] and BE[3:0] after the command phase and at the end of the data transaction.

* The data is valid when WR_N and RXF_N are both active.

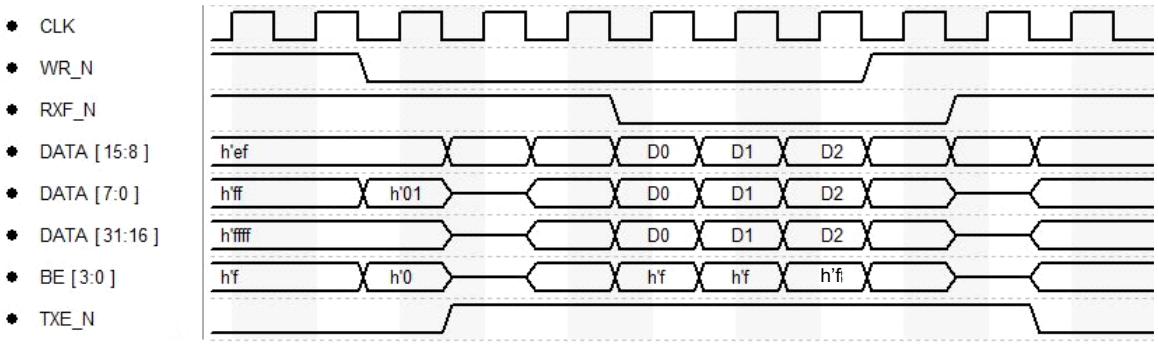


Figure 4.2 FT601 Multi-Channel FIFO mode master read transaction 2

*In Multi-channel FIFO mode master read operation, the bus master shall be able to read out the maximum possible data in the RX FIFO in one read transaction, i.e. when the FT600 or FT601 is configured in the 1 channel Multi-channel FIFO mode, the bus master shall be able to read out 4 KB in one bus transaction, and 2 KB or 1 KB in respect to the 2 channel or 4 channel mode. In write operation, if the bus master expects the data to be transferred over USB bus in the maximum possible packet length, it should write the data to the FIFO in a single bus transaction.

Please refer to the FT601 and FT600 application notes for alternate configurations:

http://www.ftdichip.com/Support/Documents/AppNotes/AN_370_FT600_Configuration_Programmer_User_Guide.pdf

E.g. Consider a USB 3.0 super-speed connection with a packet size is 1 KB, and a FIFO size of 4 KB.

Case #1: If the bus master completes a 4KB write in one transaction then this data will be transferred onto the USB bus in 4 full sized packets.

Case #2: If the bus master completes a 1KB write in one transaction then this data will be transferred onto the USB bus in a single packet (1 packet).

Case #3: If the bus master completes a 1025 byte write in one transaction then this data will be transferred onto the USB bus in one full sized packet with length of 1024 bytes (1KB) + one short sized packet with a length of 1 byte.

The waveform below shows a FT601 master write transaction for 14 bytes at channel 1 with the bus master terminating the transaction. There are turn-a-round cycles for DATA[15:8] after the command phase and at the end of the data transaction. The BE[3:0] shows that the lower 2 bytes in D3 are valid at the last word strobe in this transaction.

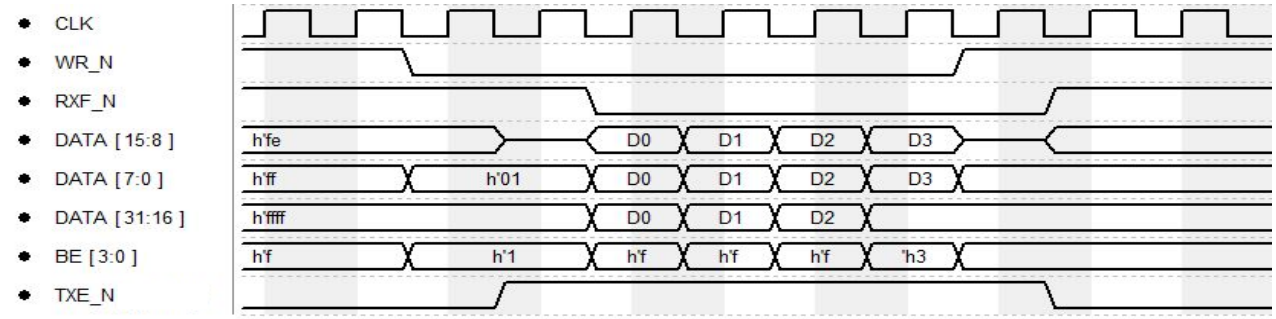


Figure 4.3 FT601 Multi-Channel FIFO mode master write transaction 1

NOTE: There is no turnaround phase for BE pins as these remain inputs when the FIFO is being written to by the master.

The waveform below shows a FT601 master write transaction where the FIFO at channel 1 uses all data space first, the RXF_N reasserts when the FIFO data space is not available after D3. There are turn-a-round cycles for DATA[15:8] after the command phase and at the end of the data transaction. The BE[3:0] shows that the transaction is all in word aligned, all 4 bytes in D3 are valid at the last word strobe in this transaction.

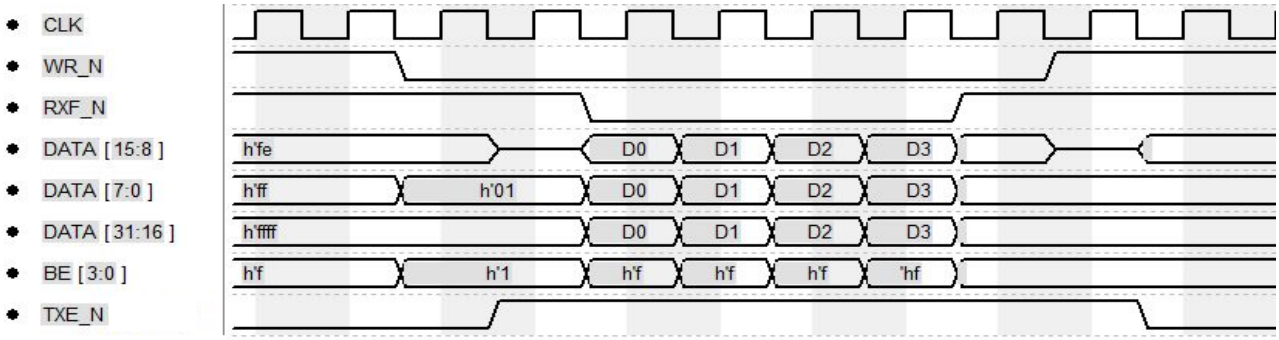


Figure 4.4 Multi-Channel FIFO mode master write transaction 2

The waveform below shows a master read of channel 1 followed by a master write to channel 1.

The channel number is selected in the command phase (DATA[7:0] = h'01 for channel 1 in this case), and data is transferred on the same data pins multiplexed to a different channel.

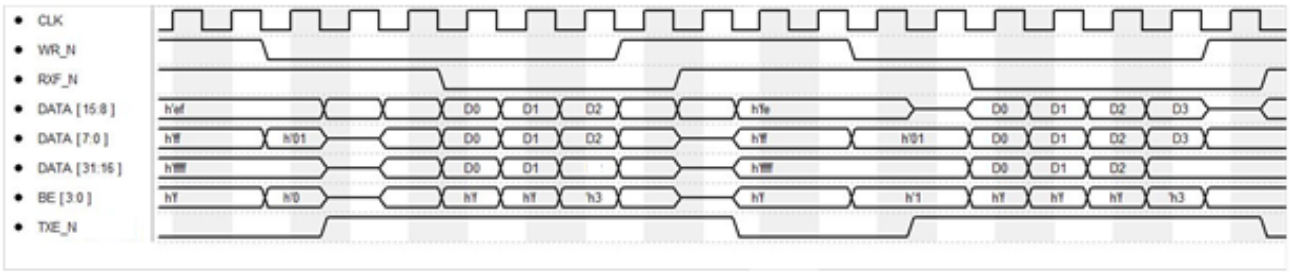


Figure 4.5 Multi-Channel FIFO mode master read followed by write transaction

4.3 245 Synchronous FIFO mode Protocols

This FT601 and FT600 slave FIFO bus uses one IN and one OUT FIFO channel while in this mode.

CLK is the clock output to the bus master; it can be configured as 66 MHz or 100 MHz

TXE_N is an output signal, Transmit FIFO Empty. It is active low and when active it indicates the Transmit FIFO has space and it is ready to receive data from the FIFO master.

RXF_N is an output signal, Receive FIFO Full. It is active low and when active it indicates the Receive FIFO has data and it is ready to be read by the FIFO master.

OE_N is an input signal, Output Enable. It is active low and when it is driven low by the bus master, the slave will drive the data and byte enable buses.

WR_N is an input signal, Write Enable. It is active low and when it is driven low by the bus master, the master has write cycle access.

RD_N is an input signal, Read Enable. It is active low and when it is driven low by the bus master, the master has read cycle access.

BE[3:0](BE[1:0] for FT600) is byte enable signal. In bus master read operation, the FT60X asserts the signal for the valid bytes in a word strobe. In bus master write operation, the bus master assets the signal for the valid bytes in a word strobe. Normally, all 4 bytes should be valid in a bus transaction except in the last word strobe when the data transaction length not aligned at word boundary.

There are 2 waveforms below to show 245 synchronous FIFO bus master write and read cycles.

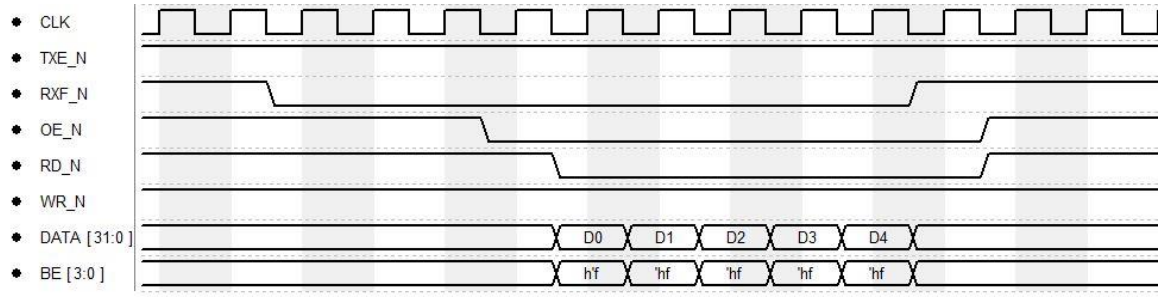


Figure 4.6 245 Synchronous FIFO mode bus master read cycle

*In 245 Synchronous FIFO mode master read operation, the bus master shall be able to read out the maximum possible data in the RX FIFO in one read transaction, i.e. the bus master shall be able to read out 4 KB in one bus transaction. In write operations, if the bus master expects the data to be transferred on the USB bus in a maximum possible packet length, it should write the data to the FIFO in a single bus transaction.

E.g. in a USB 3.0 super-speed connection, with a packet size of 1 KB, and a FIFO size of 4 KB, if the bus master completes the 4 KB in one transaction then the data will be transferred over the USB bus in 4 full sized packets. If the bus master completes 1 KB in one transaction, the data will be transferred over the

USB bus in 1 packet. If the bus master completes 1025 bytes in one transaction, the data will be transferred over USB in 1 full sized packet and one short packet with 1 byte.

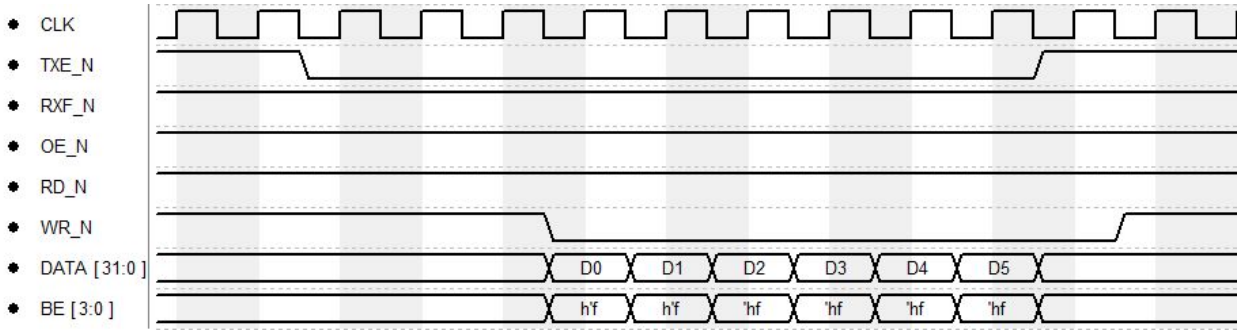


Figure 4.7 245 Synchronous FIFO mode bus master write cycle

4.4 FIFO Bus AC Timing

The FT600/FT601 device FIFO bus is a synchronous parallel bus. The CLK signal is generated by the device, with the typical FIFO clock duty cycle of 50%. Both Multi-Channel and 245 synchronous FIFO modes' worst case AC timing are shown in Figure 4.8 and Table 4.2.

In this figure, 'Input Data' includes all control signals and data lines driven by the FIFO master. 'Output Data' includes all control signals and data lines driven by the FIFO slave - FT600/FT601.

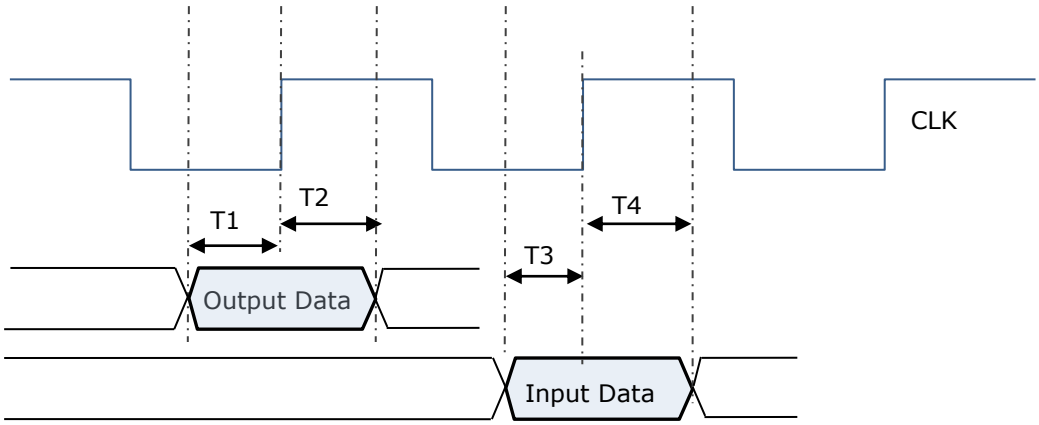


Figure 4.8 FIFO Bus AC timing diagram

Time	Description	Minimum	Maximum	Unit
T1	Slave Drive Data Set Up Time	3.0	-	ns
T2	Slave Drive Data Hold Time	3.5	-	ns
T3	Master Drive Data Set Up Time	1	-	ns
T4	Master Drive Date Hold Time	4.8	-	ns

Table 4.2 FIFO Bus AC timing

4.5 Crystal requirements

The FT60x device requires an external clock source to control the internal circuitry.

The recommended parameters for the crystal are: 30MHz ±20ppm Crystal 18pF 50 Ohm -40°C ~ 85°C. The crystal should be connected across the XI and XO pins.

Note: It is not possible to replace the crystal with an oscillator or other clock source by tying XO to GND.

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT60x devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C
VCC33/VDDA Supply Voltage	-0.3 to +4.6	V
VCCIO Supply Voltage	-0.3 to +4.0	V
VD10 Core Supply Voltage	-0.5 to +1.4	V
AVDD PLL Supply Voltage	-0.5 to +1.4	V
IOs DC Input Voltage	-0.5 to +VCCIO+0.5	V

Table 5.1 Absolute Maximum Ratings

5.2 ESD and Latch-up Specifications

Description	Reference	Minimum	Typical	Maximum	Units
Human Body Mode (HBM)	JEDEC EIA/JESD22- A114-B, Class 2	-	±2kV	-	kV
Machine mode (MM)	JEDEC EIA/JESD22- A115-A, Class B	-	±200V	-	V
Charged Device Mode (CDM)	JEDEC EIA/ JESD22-C101-D, Class-III	-	±500V	-	V
Latch-up	JESD78, Trigger Class-II	-	±200mA	-	mA

Table 5.2 ESD and Latch-Up Specifications

5.3 DC Characteristics

5.3.1 DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC33/VDDA	VCC Operating Supply Voltage	3.0	3.3	3.6	V	
VCCIO_1	VCCIO Operating Supply Voltage	3.0	3.3	3.6	V	VCCIO=3.3V
VCCIO_2	VCCIO Operating Supply Voltage	2.3	2.5	2.7	V	VCCIO=2.5V
VCCIO_3	VCCIO Operating Supply Voltage	1.65	1.8	1.95	V	VCCIO=1.8V
VD10/AVDD	Core/PLL Operating Supply Voltage	0.9	1.0	1.1	V	
Icc_1	VCC Operating Supply Current	-	70	-	mA	Idle, SuperSpeed
Icc_2	VCC Operating Supply Current	-	65	-	mA	Idle, High Speed
Icc_3	VCC Operating Supply Current	-	185	-	mA	Active, SuperSpeed, Multi-Channel FIFO mode
Icc_3	VCC Operating Supply Current	-	4	-	mA	USB Suspend
Iccio_1	VCCIO Operating Supply Current	-	4.5	-	mA	No data transfer
Iccio_2	VCCIO Operating Supply Current		9.5		mA	Data transfer
Iccio_3	VCCIO Operating Supply Current		70		µA	USB Suspend

Table 5.3 DC Characteristics

5.3.2 DC Characteristics for I/O Interface

Parameter	Description	Min	Typ	Max	Units	Conditions
VCCIO_3.3V	VCCIO Operating Supply Voltage	3.0	3.3	3.6	V	Normal Operation
VCCIO_2.5V		2.3	2.5	2.7	V	Normal Operation
VCCIO_1.8V		1.65	1.8	1.95	V	Normal Operation
VIH		VCCIO*0.7	-	-	V	Normal Operation
VIL		-	-	VCCIO*0.3	V	Normal Operation
Iin/Iout(3.3V)	Input/output Leakage	-10	-	10	uA	Without pull-up/down
Rpu/Rpd	Input pull-up/pull down resistance	30	50	75	KΩ	Vout=0~VCCIO
Iout(VCCIO=3.3V)	Output drive strength	10	-	-	mA	Total current
Iout(VCCIO=2.5V)	Output drive strength	9.4	-	-	mA	Total current
Iout(VCCIO=1.8V)	Output drive strength	5.0	-	-	mA	Total current
Cp	Pin Capacitance	-	-	2.0	pF	

Table 5.4 DC Characteristics for I/O Interface (Except USB PHY pins)

6 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT60x. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT600Q and FT601Q package options.

All USB power configurations illustrated apply to both package options for the FT60x devices. Please refer to Section 3 for the package option pin-out and signal descriptions.

6.1 USB Bus-Powered Configuration

Note: The reference designs here are for USB 3.0 Standard B or Micro-B connectors.

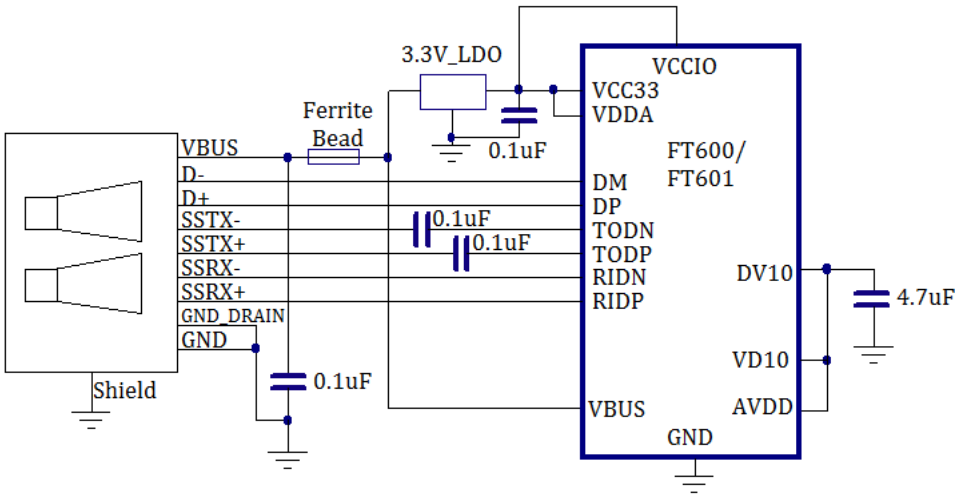


Figure 6.1 Bus-Powered Configuration-3.3V I/O

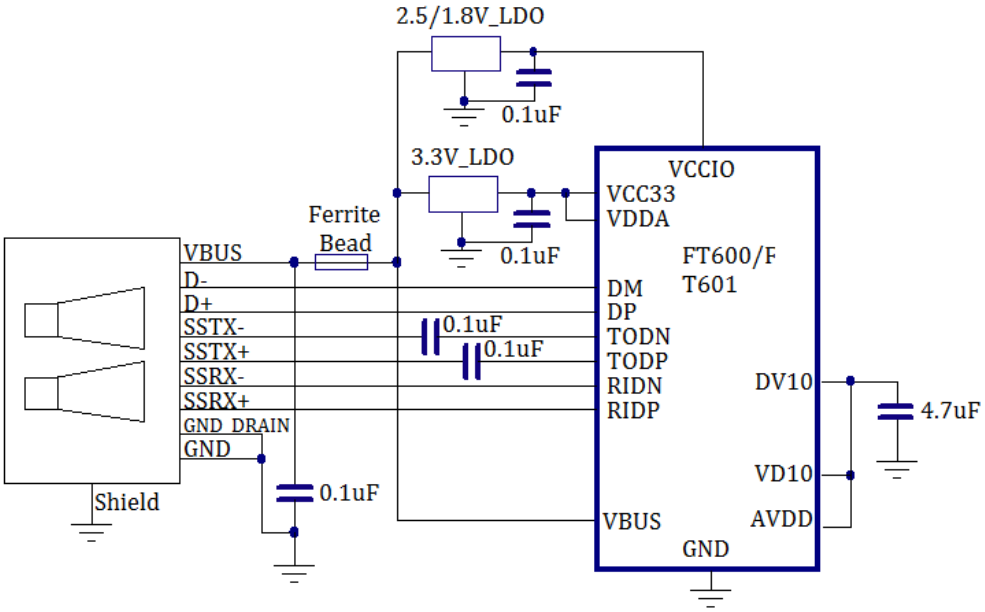


Figure 6.2 Bus-Powered Configuration-2.5V/1.8V I/O

Figure 6.1 & 6.2 illustrate the FT60x in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus via an external LDO stepping the voltage down to +3.3V.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT60x and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application.

6.2 Self-Powered Configuration

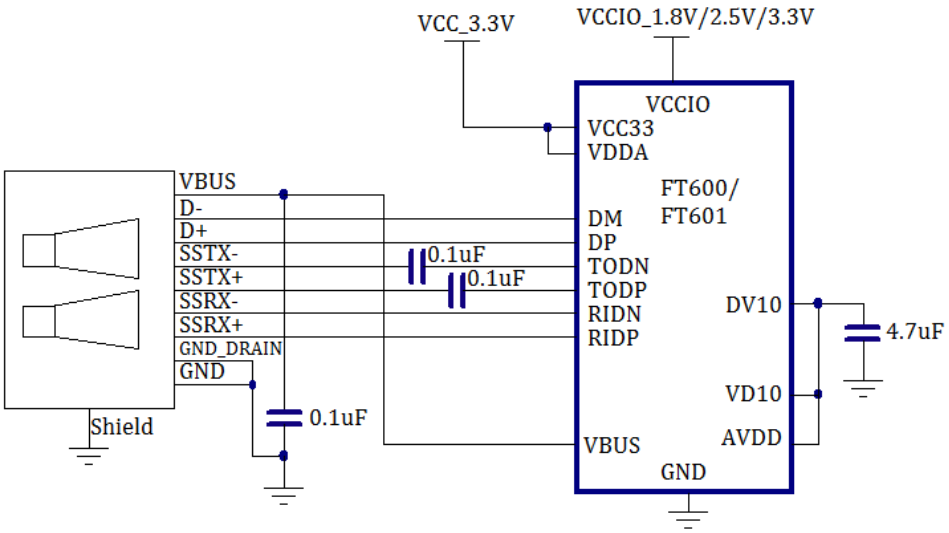


Figure 6.3 Self-Powered Configuration

Figure 6.3 illustrates the FT60x in a typical USB self-powered configuration. A USB self-powered device gets its power from its own power supply, VCC33 and VCCIO, and does not draw current from the USB bus. The basic rules for USB self-powered devices are as follows –

i) A self-powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii) A self-powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii) A self-powered device can be used with any USB host, a bus powered USB hub or a self-powered USB hub.

7 Application Example

The following sections illustrate possible applications of the FT60x. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT600Q and FT601Q package options.

7.1 FT600/FT601 Connect to FIFO Master Interface

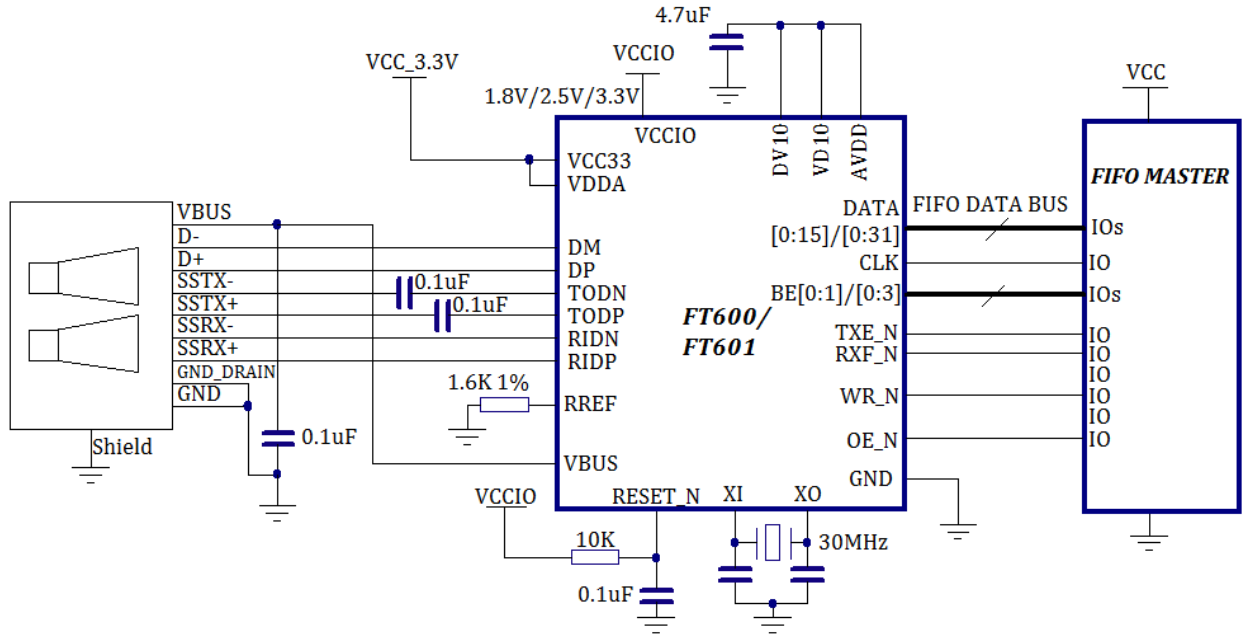


Figure 7.1 FT600/FT601 Connect to FIFO Master Interface (Multi-Channel FIFO Mode)

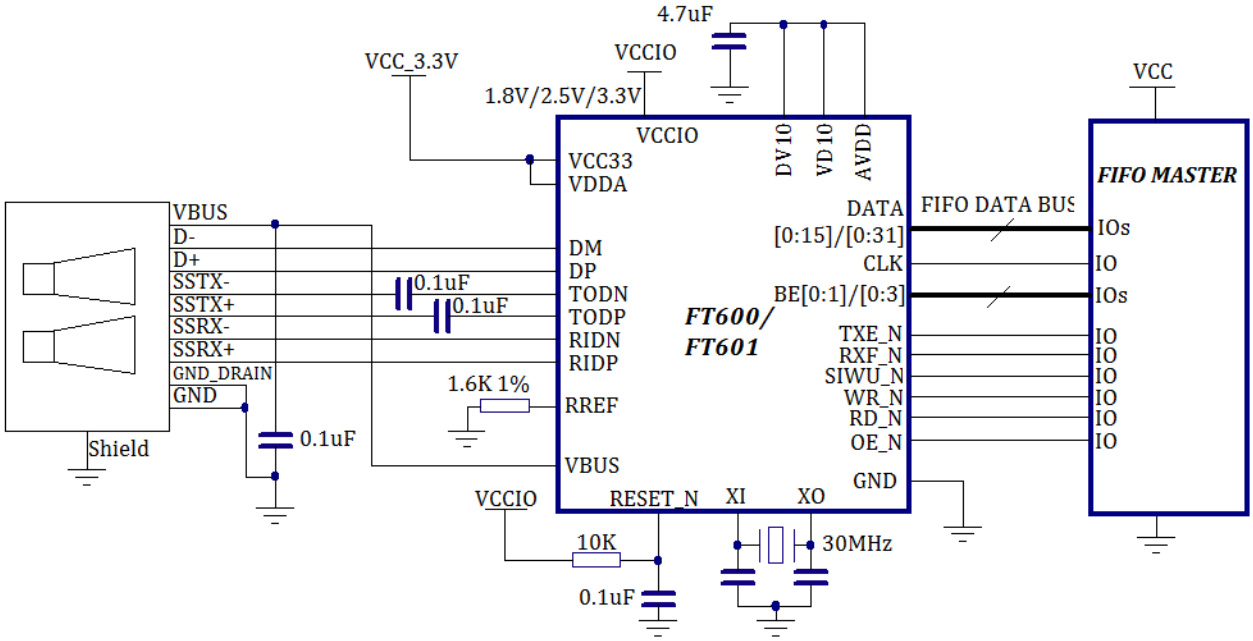


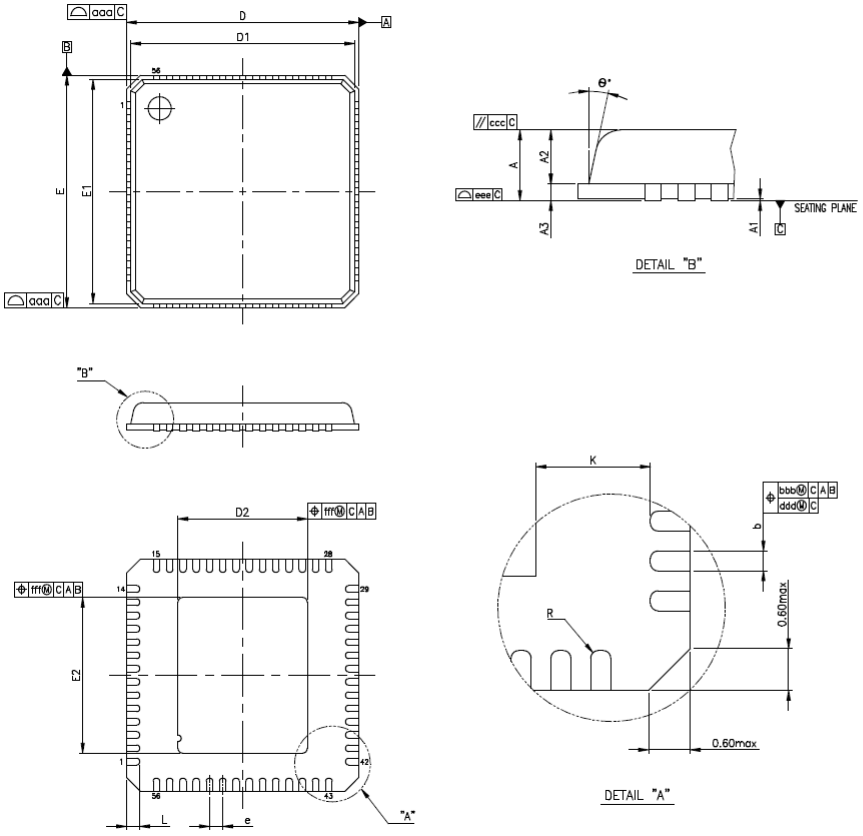
Figure 7.2 FT600/FT601 Connect to FIFO Master Interface (245 Synchronous FIFO Mode)

A typical example of using the FT600/FT601 as a USB3.0 to FIFO Master Interface is illustrated in Figure 7.1. and Figure 7.2

8 Package Parameters

The FT60x is available in two different packages based on the FIFO bus interface. The FT600Q is the QFN-56 package 16-bit FIFO bus interface and the FT601Q is the QFN-76 package 32-bit FIFO interface.

8.1 QFN-56 Package Mechanical Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	6.65	6.75	6.85
E1	6.65	6.75	6.85
e		0.40 BSC	
L	0.30	0.40	0.50
θ°	0	—	12
R	0.075	—	—
K	0.20	—	—
aaa	—	—	0.10
bbb	—	—	0.07
ccc	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
fff	—	—	0.10

UNIT : mm

		D2			E2		
	PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
⚠	161X193MIL	3.75	3.90	4.05	4.55	4.70	4.85

UNIT : mm

NOTES :
1. JEDEC : MO-220 REV.K(VKKE)
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 8.1 QFN-56 Package Dimensions

The FT600Q is supplied in a RoHS compliant 56 pin QFN package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 7.0mm x 7.0 mm body and the pins are on a 0.4 mm pitch. The above mechanical drawing shows the QFN-56 package. All dimensions are in millimetres. The centre pad on the base of the FT600Q is internally connected to GND; the PCB should connect to ground and not have signal tracking on the same layer as the chip in this area.

8.2 QFN-56 Package Markings

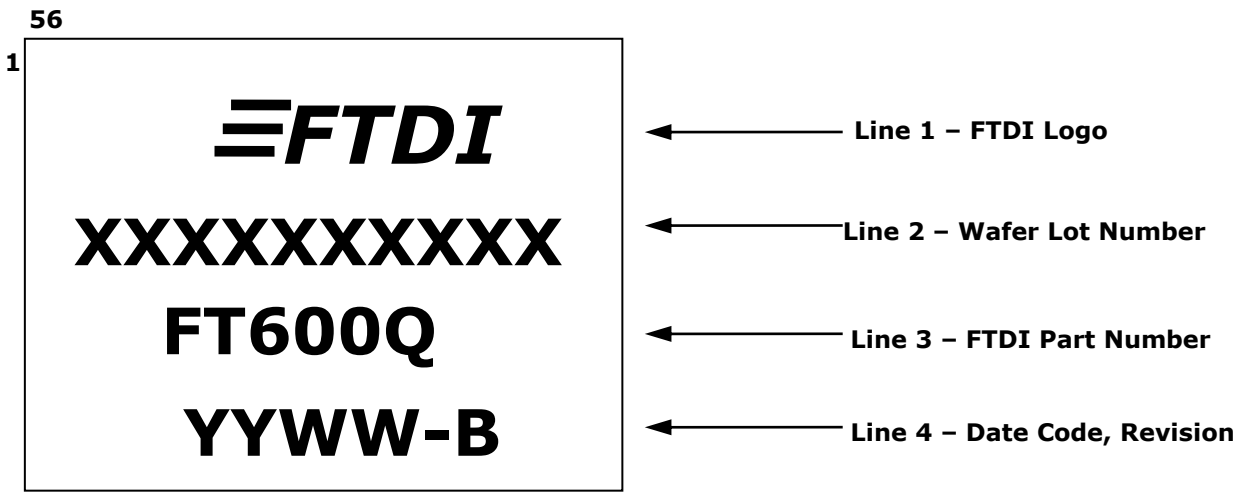
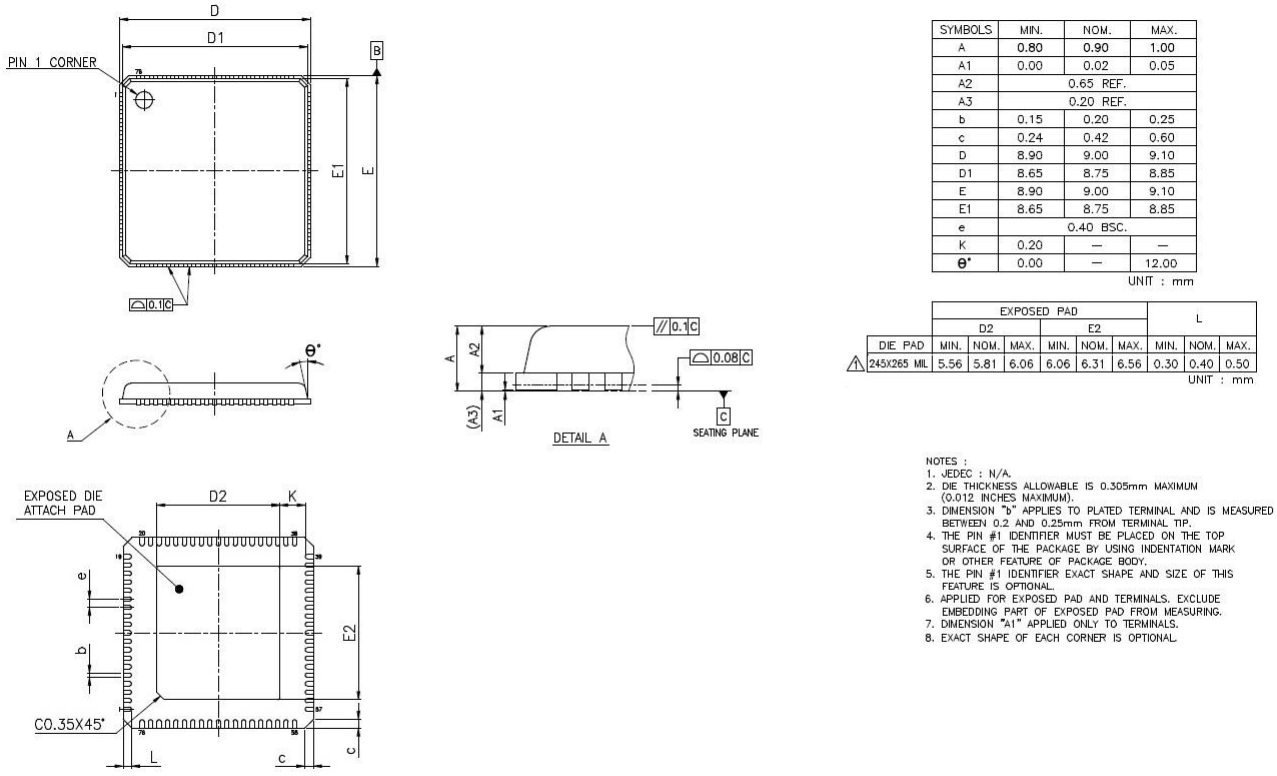


Figure 8.2 QFN-56 Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using standard font (Roman Simplex)

8.3 QFN-76 Package Mechanical Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.15	0.20	0.25
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.40 BSC.	
K	0.20	—	—
θ°	0.00	—	12.00

UNIT : mm

	EXPOSED PAD						L		
	D2			E2					
DIE PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
⚠ 245X265 MIL	5.56	5.81	6.06	6.06	6.31	6.56	0.30	0.40	0.50

UNIT : mm

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 8.3 QFN-76 Package Dimensions

The FT601Q is supplied in a RoHS compliant leadless QFN-76 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 9.0mm x 9.0mm body. The solder pads are on a 0.40mm pitch. The above mechanical drawing shows the QFN-76 package.

The centre pad on the base of the FT601Q is internally connected to GND, the PCB should connect to ground and not have signal tracking on the same layer as chip in this area.

8.4 QFN-76 Package Markings

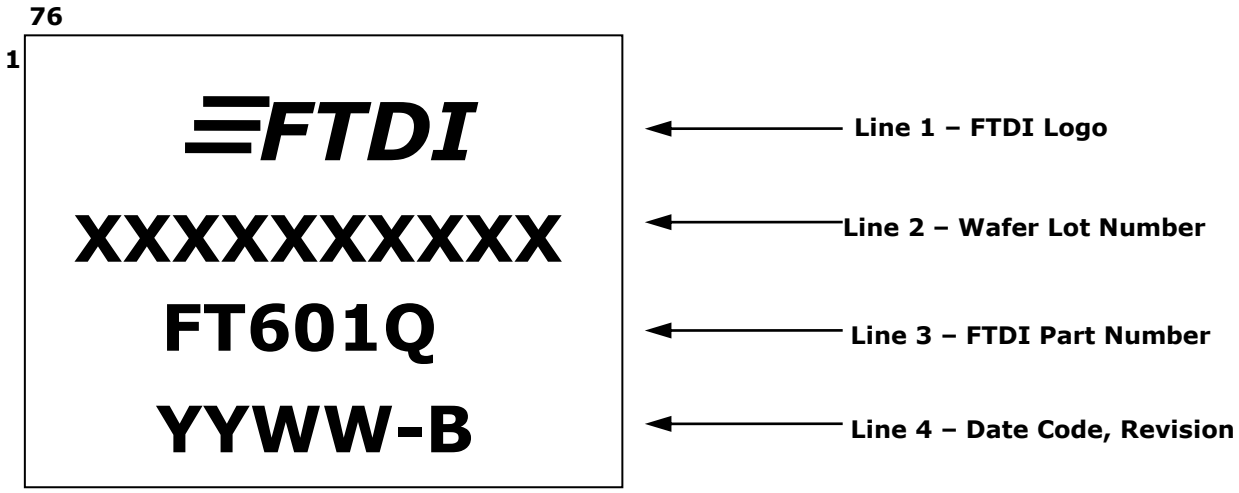


Figure 8.4 QFN-76 Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using Greatek standard font (Roman Simplex)

8.5 Solder Reflow Profile

	Ave Ramp up rate(T)	Holding Time	Peak Temp.	Liquidus Temp.	Time Above Temp.	Ave Cooling rate(T)	Result
Boundary	220.00-260.00 C	150.00-200.00 C	-------	217.00 C	255.00 C	260.00-217.00 C	
Range	0.00-3.00 (C/sec)	60.00-120.00 (sec)	260.00-265.00 (C)	60.00-150.00 (sec)	30.00-40.00 (sec)	6.00-0.00 (C/sec)	
sensor1	0.54	98.00	260.90	110.00	30.00	1.87	OK

Figure 8.5 Solder Reflow Profile

9 Contact Information

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

Useful Application Notes

AN_370 - FT600 Configuration Programmer User Guide

AN_379 D3XX Programmers Guide

AN_375 FT600 Data Loopback Application User Guide

Modules Datasheet

DS_UMFT60xx module datasheet

Data Loopback Application

FT600DataLoopback

Acronyms and Abbreviations

Terms	Description
ADC	Analog To Digital Converter
BCD	Binary Coded Decimal
DAC	Digital To Analog Converter
ESD	Electro Static Discharge
FIFO	First In First Out
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
LDO	Low Drop Out regulator
PLD	Programmable Logic Device
QFN	Quad Flat Non-leaded package
RoHS	Restriction of Hazardous Substances Directive
USB	Universal Serial Bus
VQFN	Very Thin Quad Flat Non-Leaded Package

Appendix B – List of Figures and Tables

List of Figures

List of Tables

Appendix C – Revision History

Document Title: FT600Q-FT601Q IC Datasheet (USB 3.0 to FIFO Bridge)
Document Reference No.: FT_001118
Clearance No.: FTDI#424
Product Page: http://www.ftdichip.com/FTProducts.htm
Document Feedback: Send Feedback

Revision	Changes	Date
Version 1.0	Initial Release	2015-07-07
Version 1.01	Updated Figure 4.7 & Table 3.1	2015-09-08
Version 1.02	Revised Release	2016-02-03
Version 1.03	Update Fig 8.3; Update to FT601/FT600 Rev B	2016-08-24
Version 1.04	Updated Ordering information, and package marking for rev B. Updated MAC/Linus driver status and Added Win10 into driver support list Added section 4.5 on crystals	2016-10-17
Version 1.05	Table 4.2 has been updated with new timing values.	2017-11-03

Revision History

Revision history (internal use only, please clearly state all changes here before saving the file)

Revision	Date YYYY-MM-DD	Changes	Editor
Draft	2014-09-29	Initial Datasheet Created	Samuel
Draft 0.1	2014-03-11	1.change block diagram 2.change pin out name	Samuel
Draft 1.0	2014-05-11	1. change block diagram, add in NVM and BCD blocks 2. Add in details description for FIFO protocol. 3. Corrected section 5.3.2, 6 and 7. 4. section 5.1 add in Ios Input voltage rating 5. Add in FT600 IC image.	Samuel
Draft 1.0	2014-05-11	First review and comments	G Lunn
Draft 1.0	2014-05-11	Reviewed and comments attached. Minor typos corrected.	R Bienek
Draft 1.0	2014-06-11	1. corrected block diagram 2. corrected section 8 Package Mechanical Dimensions 3. Corrected section 3.4 protocols waveform. 4. corrected section 1.1 driver support	Samuel
Draft 1.0	2014-06-11	Reviewed. Still some open comments and figure 2.1 spelling of "controller" is getting closer but still needs fixed	G Lunn
Draft 1.0	2014-06-11	1.corrected spelling of "controller" in figure 2.1 2.change 245 FIFO to "245 synchronous FIFO" 3.change FT245 to 245 in section 4	
Draft 1.0	2014-06-11	Reviewed. Should be OK for an early release. As we are not launching the product yet it may be prudent to watermark the pdf with "subject to change"	G Lunn
Version Draft	2014-07-11	Reviewed and approved by LCE and PH to be released as draft version, including 'Subject to change' watermark	S Glasgow
Draft 1.1	2015-04-15	Add in section 3.5 FIFO bus AC timing	Samuel
Draft 1.2	2015-04-17	1. change sention3.3 /3.4 to section 4.2/4.3 2. Change FIFO bus AC timing diagram, add in	Samuel

		explain and timing table 3.add in 5.2 ESD and Latch-up Specifications data 4. Update Figure and Table list	
Draft 1.2	2015-04-21	Reviewed, commented, minor edits Updated footers, section 1.1, section 1.2	G Lunn
Draft1.2	2015-05-29	Updated section4.1,4.2	Jiang Qian
Version 1.0	2015-06-11	Updated section4.1, Appendix B, updated header Version Draft to Version 1.0	Samuel
Version 1.0 (SharePoint 0.2)	2015-06-11	Minor update, update document info/clearance number and some comments related issues	Jiang Qian
Version 1.0 (SharePoint 0.2)	2015-06-11	Reviewed, minor edits and comments.	G Lunn
Version 1.0 (SharePoint 0.8)	2015-06-18	Updated section 6, section 7 diagrams. Appendix B	Samuel
Version 1.0 (SharePoint 0.8)	2015-06-18	Reviewed and Some comments	Paul Huang
Version 1.0	2015-06-18	Reviewed updates - some comments still to be closed	G Lunn
Version 1.0 (SharePoint 0.13)	2015-07-03	Update document after discussion with Gordon L. Update diagrams with some typo. Put SIWU_N as reserved since not used in design. Update the BE function in 245 mode. Removed the document reference of DFU/Config, replace with API user manual and demo application user manual which are in the release package	Jiang Qian
Version 1.0 (SharePoint 0.13)	2015-07-03	Reviewed. Recommend for approval	G Lunn
Version 1.0	2015-07-07	Approved LCE	G Lunn
Version 1.1 Draft 0.1	2015-07-09	Update the diagram of Figure 4.7 245 Synchronous FIFO mode bus master write cycle (Corrected typo of duplicated “D4”).	Jiang Qian
Version 1.01	2015-07-10	Reviewed recommend for approval	G Lunn
Version 1.01	2015-07-16	Approved LCE	G Lunn

Version 1.01	2015-09-02	Corrected the Product page hyperlink under Appendix C – Revision History Section as per Amanda Punzalan feedback ((earlier the link was pointing to MCU page on the FTDI Website. Now it points to the Product page)	L Subramanian
Version 1.01	2015-09-08	Updated the typo in table 3.1 (as per Bug Id 374)	L Subramanian
Version 1.02	2015-10-20	Corrected the wording / type identified by customer. Refer to Bug 387	L Subramanian
Version 1.02	2015-11-16	Removed FIFO Clock out frequency option 66.67MHz (Section 4.1 Key Features & Function Description -> FIFO Bus Clock option) since it is not officially supported (Refer to Bug ID 394)	L Subramanian
Version 1.02	2015-12-08	Reviewed, just waiting for reflow profile to be added	G Lunn
Version 1.02	2015-12-23	Solder Reflow Profile added	C Martin
Version 1.03	2016-02-03	Verified the document for standard template and updated wherever applicable Added Acronyms & Abbreviation table as part of Appendix A Approved LCE	L Subramanian
Version 1.03	2016-03-23	Removed incorrect information from Fig 8.3	Alan Yang
Version 1.03	2016-06-16	Removed the word "Datasheet" that was repeating twice on the header	L Subramanian
Version 1.03	2016-07-25	Update FT600 and FT601 chip Rev B (should obsolete Rev A chips)	Jiang Qian
Version 1.03	2016-08-02	Reviewed Corrected TW contact details Closed what comments I could – none of the images were changed to rev B – don't think it is necessary Why rev 1.04? 1.03 was never released.	G Lunn
Version 1.03	2016-08-24	Updated the document version in the Send Feedback hyperlink Approved LCE	L Subramanian
Version 1.04	2016-10-02	Update Ordering information, and package marking for rev B.	Paul Huang
Version 1.04	2016-10-04	Update MAC/Linus driver status and Add Win10 into driver support list	Paul Huang
Version 1.04	2016-10-05	Added section 4.5 on crystals Reviewed other edits Recommend for approval	G Lunn

Version 1.04	2016-10-17	Approved LCE	L Subramanian
Version 1.05	2017-10-25	Table 4.2 has been updated with new timing values.	Arun Pappan
Version 1.05	2017-10-25	Reviewed. Closes bug ID 62/100 Recommend for approval	G Lunn
Version 1.05	2017-11-03	Approved LCE	L Subramanian