MC78L00A Series, NCV78L00A

100 mA Positive Voltage Regulators

The MC78L00A Series of positive voltage regulators are inexpensive, easy−to−use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode−resistor combination, as output impedance and quiescent current are substantially reduced.

Features

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00A Series)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

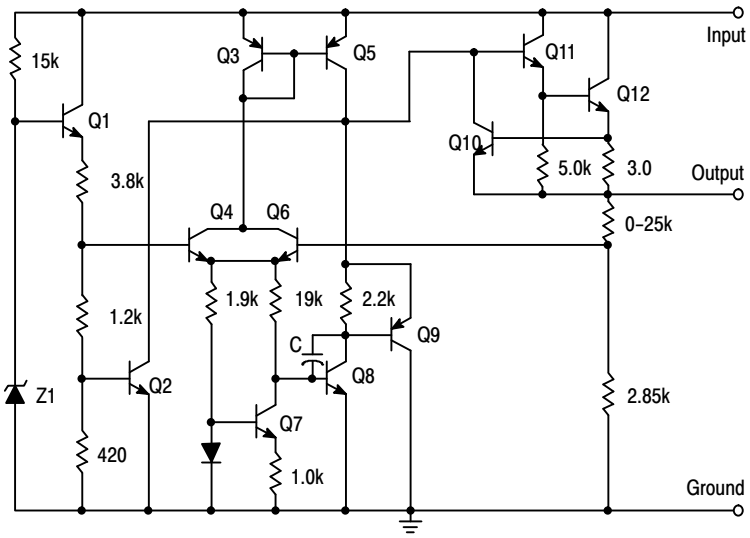

Figure 1. Representative Schematic Diagram

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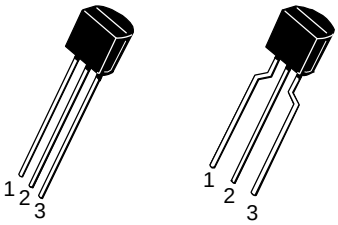


STRAIGHT LEAD BULK PACK

BENT LEAD TAPE & REEL AMMO PACK

TO−92
P SUFFIX
CASE 029

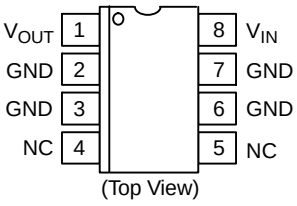
Pin: 1. Output
2. Ground
3. Input

SOIC−8*
D SUFFIX
CASE 751

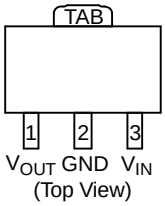
SOT−89
CASE 528AG

*SOIC−8 is an internally modified SO−8 package. Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOIC−8 conforms to all external dimensions of the standard SO−8 package.

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 12 of this data sheet.

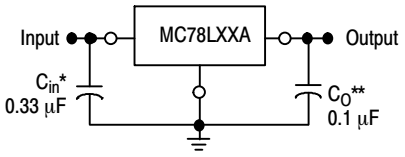


Figure 2. Standard Application

A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability; however, it does improve transient response.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (5.0 V−9.0 V) (12 V−18 V) (24 V)	V_I	30 35 40	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Maximum Junction Temperature	T_J	150	°C
Moisture Sensitivity Level	MSL	1	−
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD Charged Device Model tested per EIA/JES D22/C101, Field Induced Charge Model.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Package Dissipation	PD	Internally Limited	W
Thermal Characteristics, TO−92 Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W
Thermal Characteristics, SOIC8 Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	Refer to Figure 8	°C/W
Thermal Characteristics, SOT−89 Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	55	°C/W

2. Thermal Resistance, Junction−to−Ambient depends on P.C.B. Copper area. See details in Figure 8.

Thermal Resistance, Junction−to−Case is not defined. SOIC 8 lead and TO-92 packages that do not have a heat sink like other packages may have. This is the reason that a Theta JC is never specified. A little heat transfer will occur through the package but since it is plastic, it is minimal. The majority of the heat that is transferred is through the leads where they connect to the circuit board.

ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, −40°C < T_J < +125°C (for MC78LXXAB, NCV78L05A), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

		MC78L05AC, AB, NCV78L05A			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 – –	 55 45	 150 100	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.75 4.75	 – –	 5.25 5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.8 –	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 Vdc ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

NOTE: NCV78L05A: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, −40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

		MC78L08AC, AB			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 10.5 Vdc ≤ V_I ≤ 23 Vdc 11 Vdc ≤ V_I ≤ 23 Vdc	Reg_{line}	 – –	 20 12	 175 125	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 15 8.0	 80 40	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 7.6 7.6	 – –	 8.4 8.4	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.0 –	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 15 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, −40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

		MC78L09AC, AB			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage (T_J = +25°C)	V_O	8.6	9.0	9.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 11.5 Vdc ≤ V_I ≤ 24 Vdc 12 Vdc ≤ V_I ≤ 24 Vdc	Reg_{line}	 – –	 20 12	 175 125	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 15 8.0	 90 40	mV
Output Voltage (11.5 Vdc ≤ V_I ≤ 24 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 15 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 8.5 8.5	 – –	 9.5 9.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.0 –	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 13 V ≤ V_I ≤ 24 V, T_J = +25°C)	RR	37	57	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, −40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

		MC78L12AC, AB			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C, I_O = 40 Ma) 14.5 Vdc ≤ V_I ≤ 27 Vdc 16 Vdc ≤ V_I ≤ 27 Vdc	Reg_{line}	 – –	 120 100	 250 200	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 20 10	 100 50	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 11.4 11.4	 – –	 12.6 12.6	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 4.2 –	 6.5 6.0	mA
Input Bias Current Change (16 Vdc ≤ V_I ≤ 27 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, −40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

		MC78L15AC, AB / NCV78L15A			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 17.5 Vdc ≤ V_I ≤ 30 Vdc 20 Vdc ≤ V_I ≤ 30 Vdc	Reg_{line}	 – –	 130 110	 300 250	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 25 12	 150 75	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 14.25 14.25	 – –	 15.75 15.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 4.4 –	 6.5 6.0	mA
Input Bias Current Change (20 Vdc ≤ V_I ≤ 30 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C, unless otherwise noted.)

		MC78L18AC			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 21.4 Vdc ≤ V_I ≤ 33 Vdc 20.7 Vdc ≤ V_I ≤ 33 Vdc 22 Vdc ≤ V_I ≤ 33 Vdc 21 Vdc ≤ V_I ≤ 33 Vdc	Reg_{line}	 – –	 45 35	 325 275	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 30 15	 170 85	mV
Output Voltage (21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 17.1 17.1	 – –	 18.9 18.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.1 –	 6.5 6.0	mA
Input Bias Current Change (22 Vdc ≤ V_I ≤ 33 Vdc) (21 Vdc ≤ V_I ≤ 33 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C, unless otherwise noted.)

		MC78L24AC			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 27.5 Vdc ≤ V_I ≤ 38 Vdc 28 Vdc ≤ V_I ≤ 80 Vdc 27 Vdc ≤ V_I ≤ 38 Vdc	Reg_{line}	 – – –	 – 50 60	 – 300 350	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 40 20	 200 100	mV
Output Voltage (28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (28 Vdc ≤ V_I = 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA) (27 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 22.8 22.8	 – –	 25.2 25.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.1 –	 6.5 6.0	mA
Input Bias Current Change (28 Vdc ≤ V_I ≤ 38 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

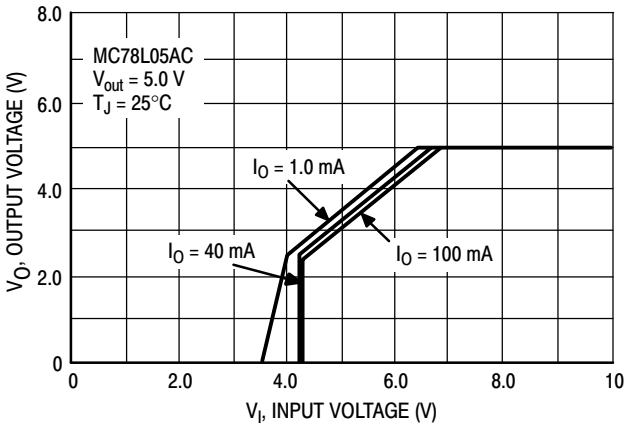


Figure 3. Dropout Characteristics

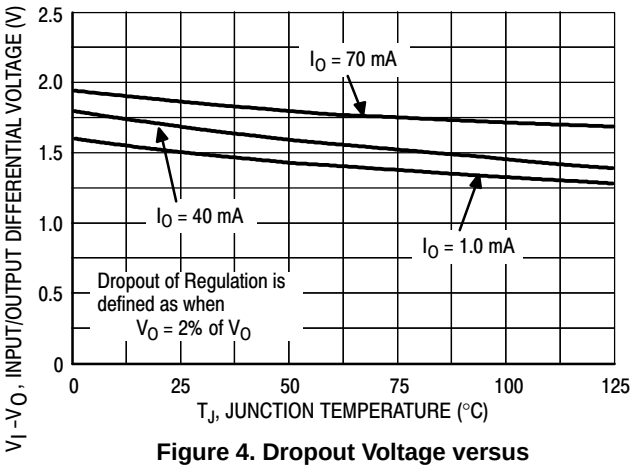


Figure 4. Dropout Voltage versus Junction Temperature

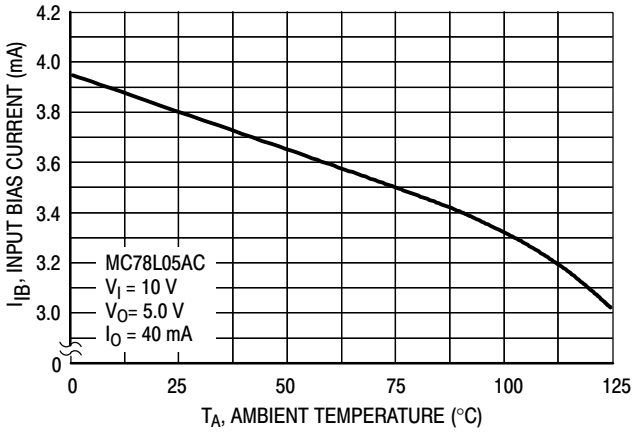


Figure 5. Input Bias Current versus Ambient Temperature

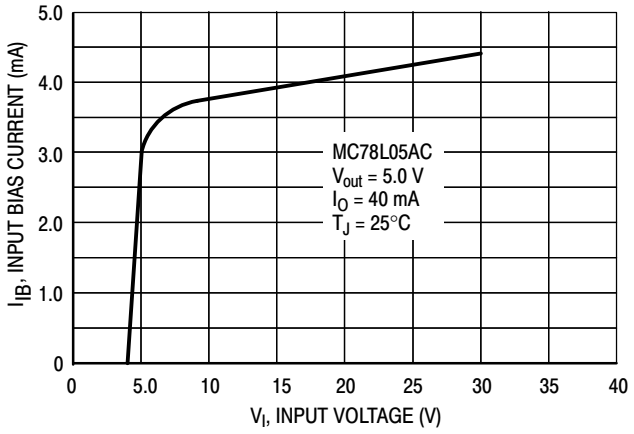


Figure 6. Input Bias Current versus Input Voltage

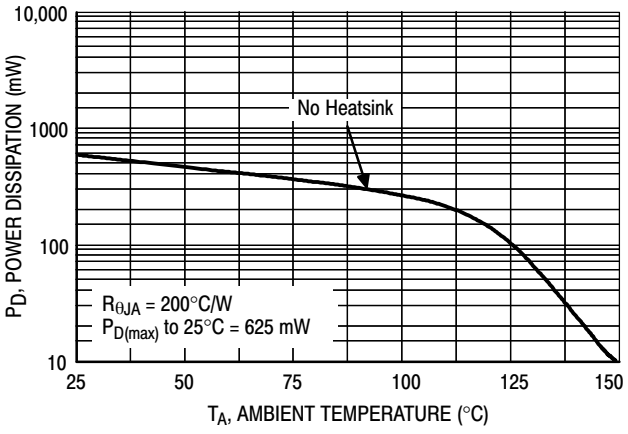


Figure 7. Maximum Average Power Dissipation versus Ambient Temperature − TO−92 Type Package

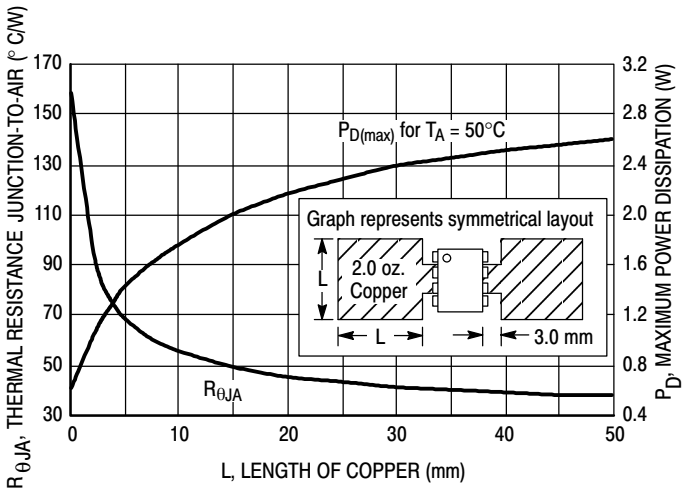


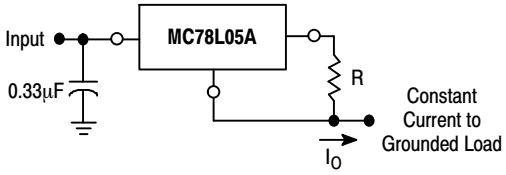
Figure 8. SOIC−8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

APPLICATIONS INFORMATION

Design Considerations

The MC78L00A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high−frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50 Ω, 1/2 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 9. Current Regulator

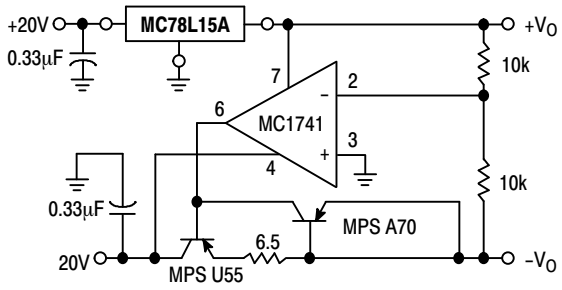


Figure 10. ±15 V Tracking Voltage Regulator

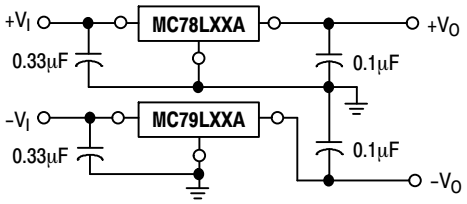


Figure 11. Positive and Negative Regulator

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package	Shipping†
MC78L05ABDG	5.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
NCV78L05ABDG*	5.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L05ABDR2G	5.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV78L05ABDR2G*	5.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L05ABPG	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
NCV78L05ABPG*	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L05ABPRAG	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
NCV78L05ABPRAG*	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L05ABPREG	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
NCV78L05ABPREG*	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L05ABPRMG	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
NCV78L05ABPRMG*	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
NCV78L05ABPRPG*	5.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L05ACDG	5.0 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L05ACDR2G	5.0 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L05ACPG	5.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L05ACPRAG	5.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L05ACPREG	5.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L05ACPRMG	5.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L05ACPRPG	5.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L05ACHT1G	5.0 V	T_J = 0° to +125°C	SOT−89 (Pb−Free)	2500 / Tape & Reel
MC78L08ABDG	8.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail

*NCV78L05A, NCV78L12A, NCV78L15A: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ORDERING INFORMATION (continued)

Device	Output Voltage	Operating Temperature Range	Package	Shipping†
MC78L08ABDR2G	8.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV78L08ABDR2G*	8.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L08ABPG	8.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L08ABPRAG	8.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L08ABPRPG	8.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L08ACDG	8.0 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L08ACDR2G	8.0 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L08ACPG	8.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L08ACPRAG	8.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L08ACPREG	8.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L08ACPRPG	8.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L09ABDG	9.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L09ABDR2G	9.0 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L09ABPRAG	9.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L09ABPRPG	9.0 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L09ACDG	9.0 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L09ACDR2G	9.0 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L09ACPG	9.0 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L12ABDG	12 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L12ABDR2G	12 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV78L12ABDG*	12 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
NCV78L12ABDR2G*	12 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L12ABPG	12 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag

*NCV78L05A, NCV78L12A, NCV78L15A: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ORDERING INFORMATION (continued)

Device	Output Voltage	Operating Temperature Range	Package	Shipping†
MC78L12ABPRPG	12 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
NCV78L12ABPG*	12 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L12ACDG	12 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L12ACDR2G	12 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L12ACPG	12 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L12ACPRAG	12 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L12ACPREG	12 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L12ACPRMG	12 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L12ACPRPG	12 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L15ABDG	15 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L15ABDR2G	15 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV78L15ABDR2G*	15 V	T_J = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L15ABPG	15 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L15ABPRAG	15 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L15ABPRPG	15 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L15ACDG	15 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC78L15ACDR2G	15 V	T_J = 0° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC78L15ACPG	15 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L15ACPRAG	15 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L15ACPRPG	15 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L18ABPG	18 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L18ACPG	18 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L18ACPRAG	18 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel

*NCV78L05A, NCV78L12A, NCV78L15A: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

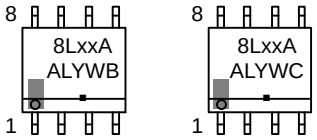
ORDERING INFORMATION (continued)

Device	Output Voltage	Operating Temperature Range	Package	Shipping†
MC78L18ACPRMG	18 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L18ACPRPG	18 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack
MC78L24ABPG	24 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
NCV78L24ABPRPG*	24 V	T_J = −40° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L24ACPG	24 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 Units / Bag
MC78L24ACPRAG	24 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Tape & Reel
MC78L24ACPRPG	24 V	T_J = 0° to +125°C	TO−92 (Pb−Free)	2000 / Ammo Pack

*NCV78L05A, NCV78L12A, NCV78L15A: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

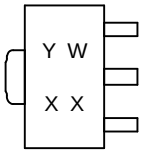
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751



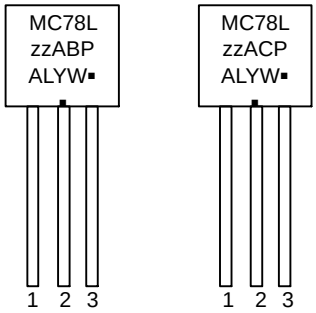
xx = 05, 08, 09, 12, or 15
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
B, C = Temperature Range
▪ = Pb−Free Package

SOT−89
CASE 528AG



Y = Year
W = Work Week
XX = Specific Device Code

TO−92
P SUFFIX
CASE 029



zz = 05, 08, 09, 12, 15, 18 or 24
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

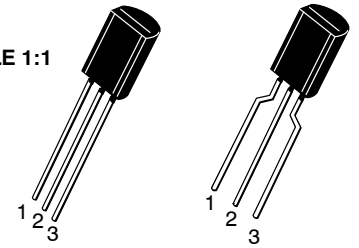
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

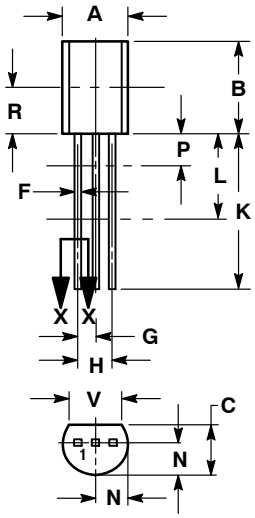
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

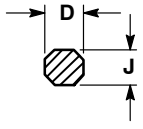
SCALE 1:1



STRAIGHT LEAD BENT LEAD



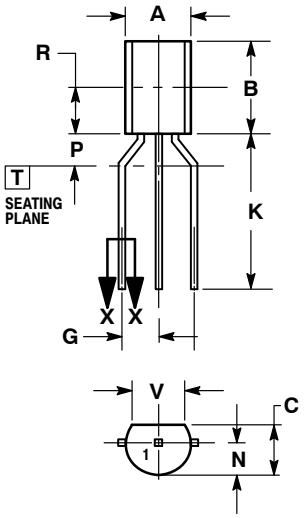
STRAIGHT LEAD



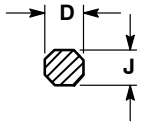
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



BENT LEAD



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 2**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

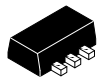
STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

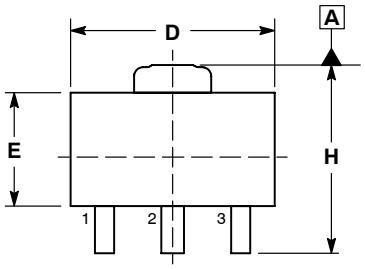
ON Semiconductor®

SOT−89, 3 LEAD
CASE 528AG
ISSUE O

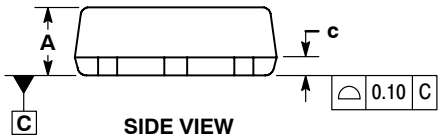
DATE 04 MAR 2014



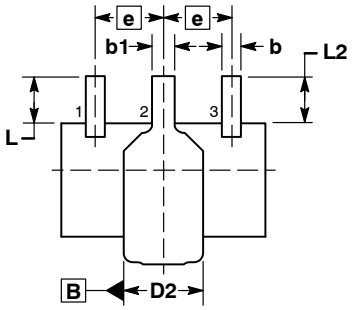
SCALE 2:1



TOP VIEW



SIDE VIEW

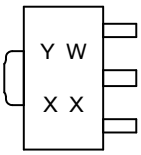


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSIONS L, L2, D2, AND H ARE MEASURED AT DATUM PLANE C.
6. CENTER LEAD CONTOUR MAY VARY WITHIN THE REGION DEFINED BY DIMENSION E.
7. DIMENSION D2 IS DEFINED AT ITS WIDEST POINT.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
b	0.38	0.47
b1	0.46	0.55
c	0.40	0.44
D	4.40	4.60
D2	1.60	1.90
E	2.40	2.60
e	1.50 BSC	
H	4.05	4.25
L	0.89	1.20

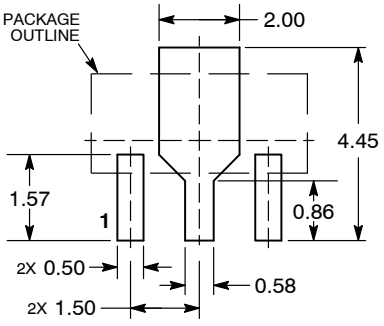
GENERIC MARKING DIAGRAM*



Y = Year
W = Work Week
XX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**SOT−89, 3 LEAD**	**PAGE 1 OF 1**

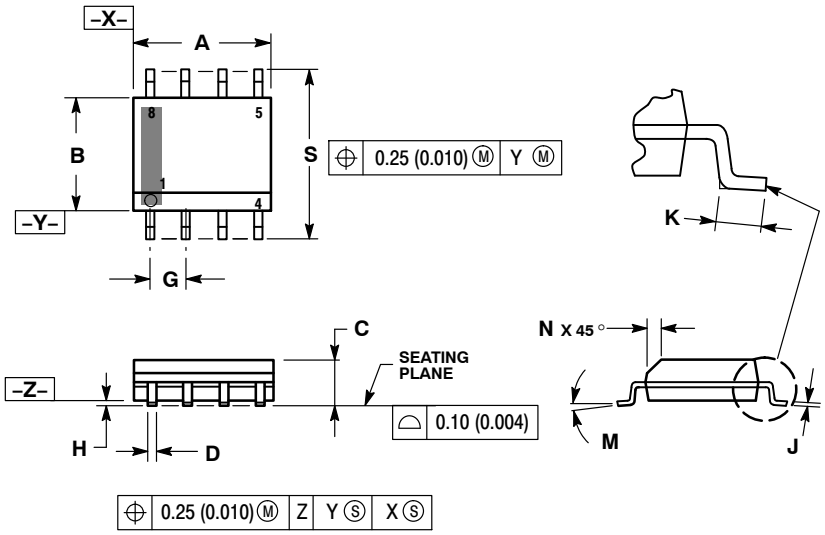
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

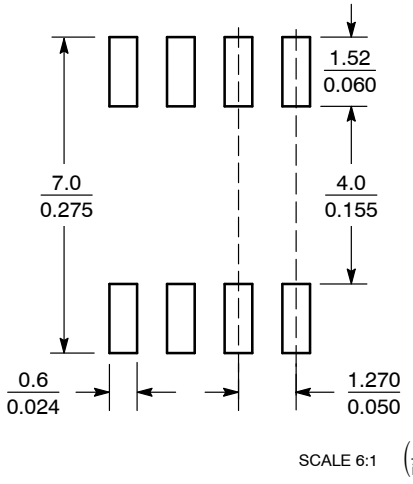
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

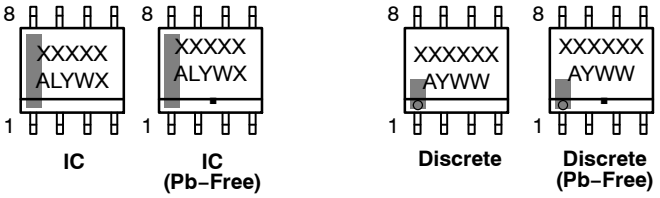
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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